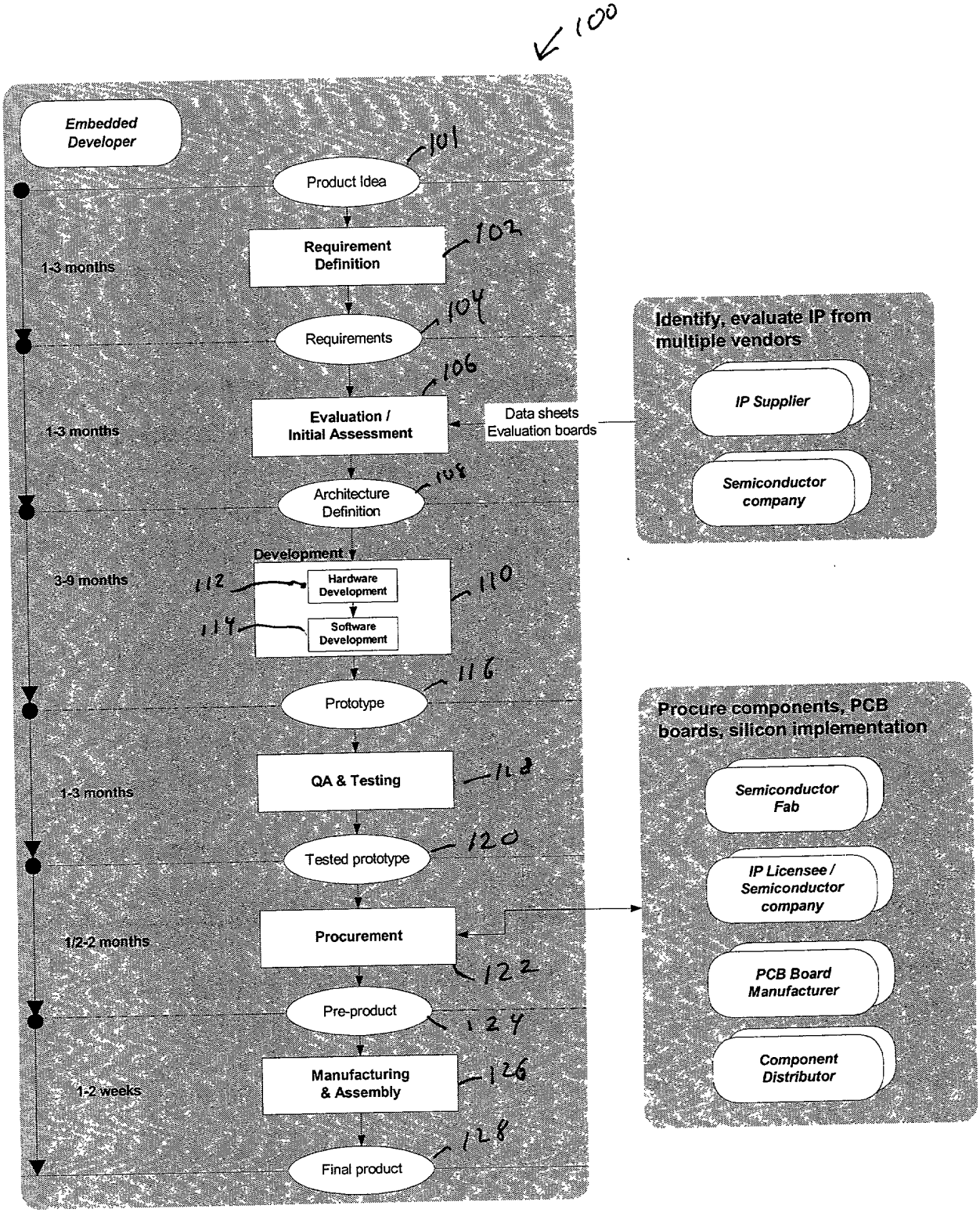


FIG. 1. (prior art)

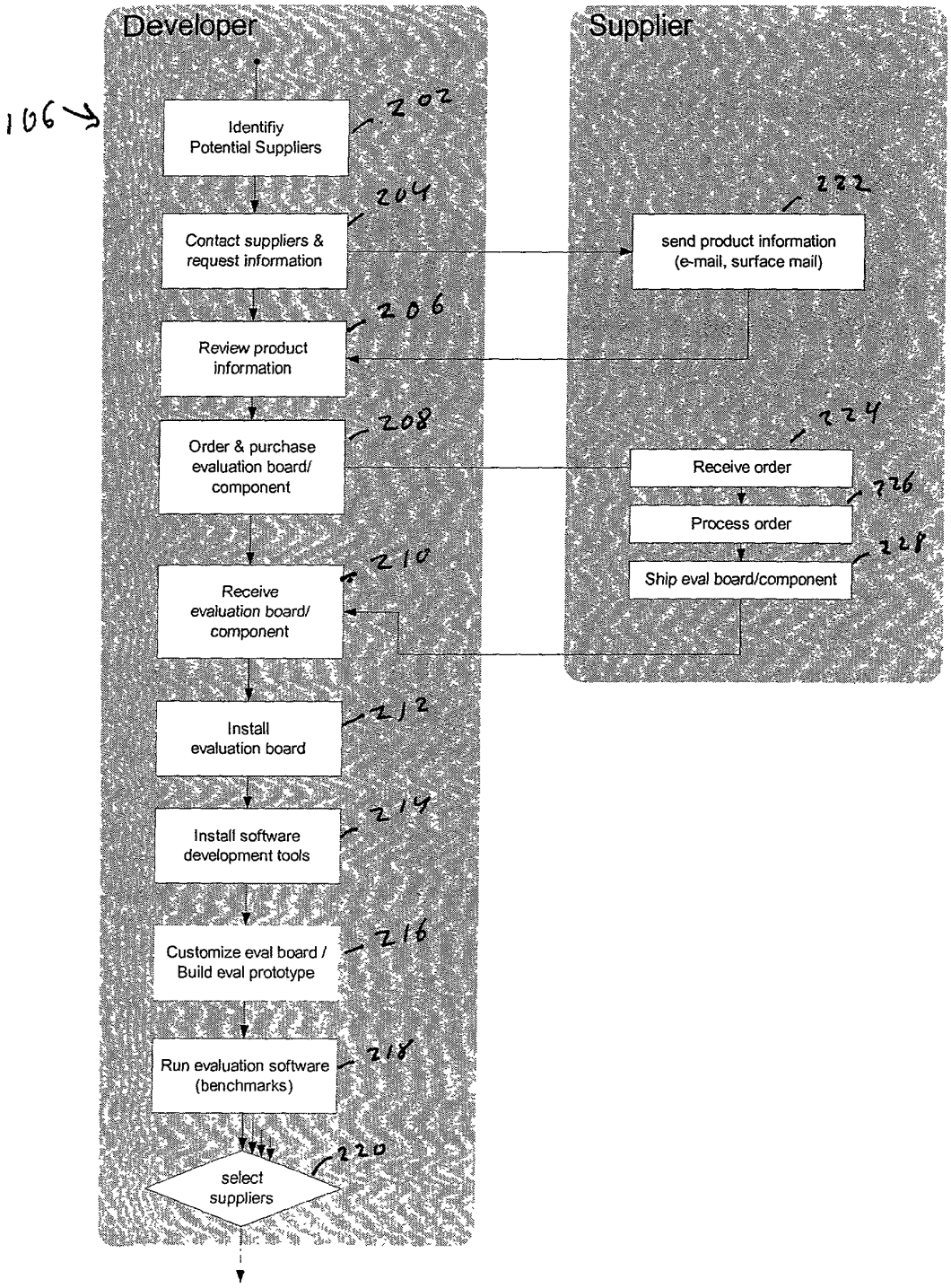


FIG. 2 (prior art)

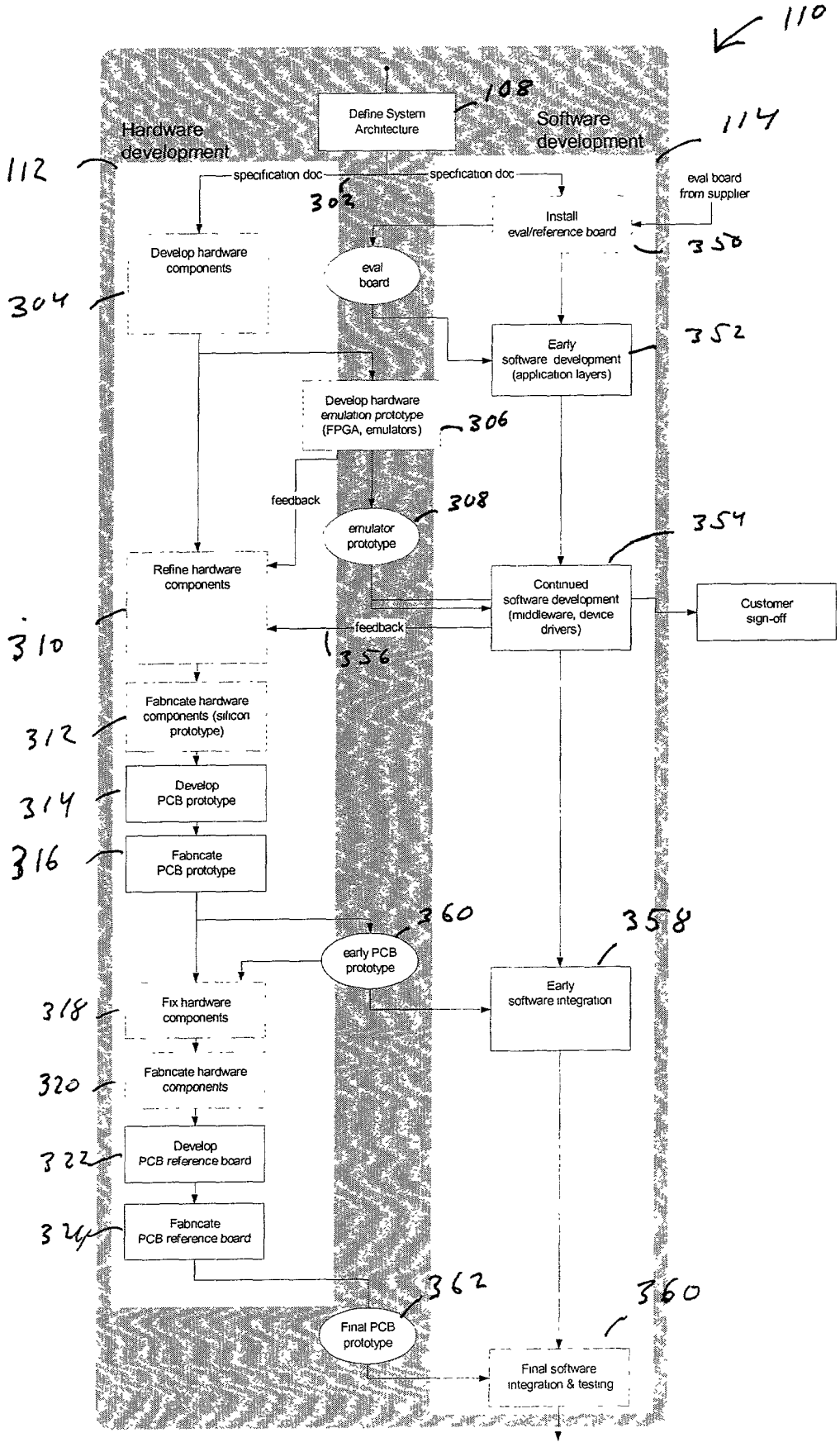


FIG. 3 (prior art)

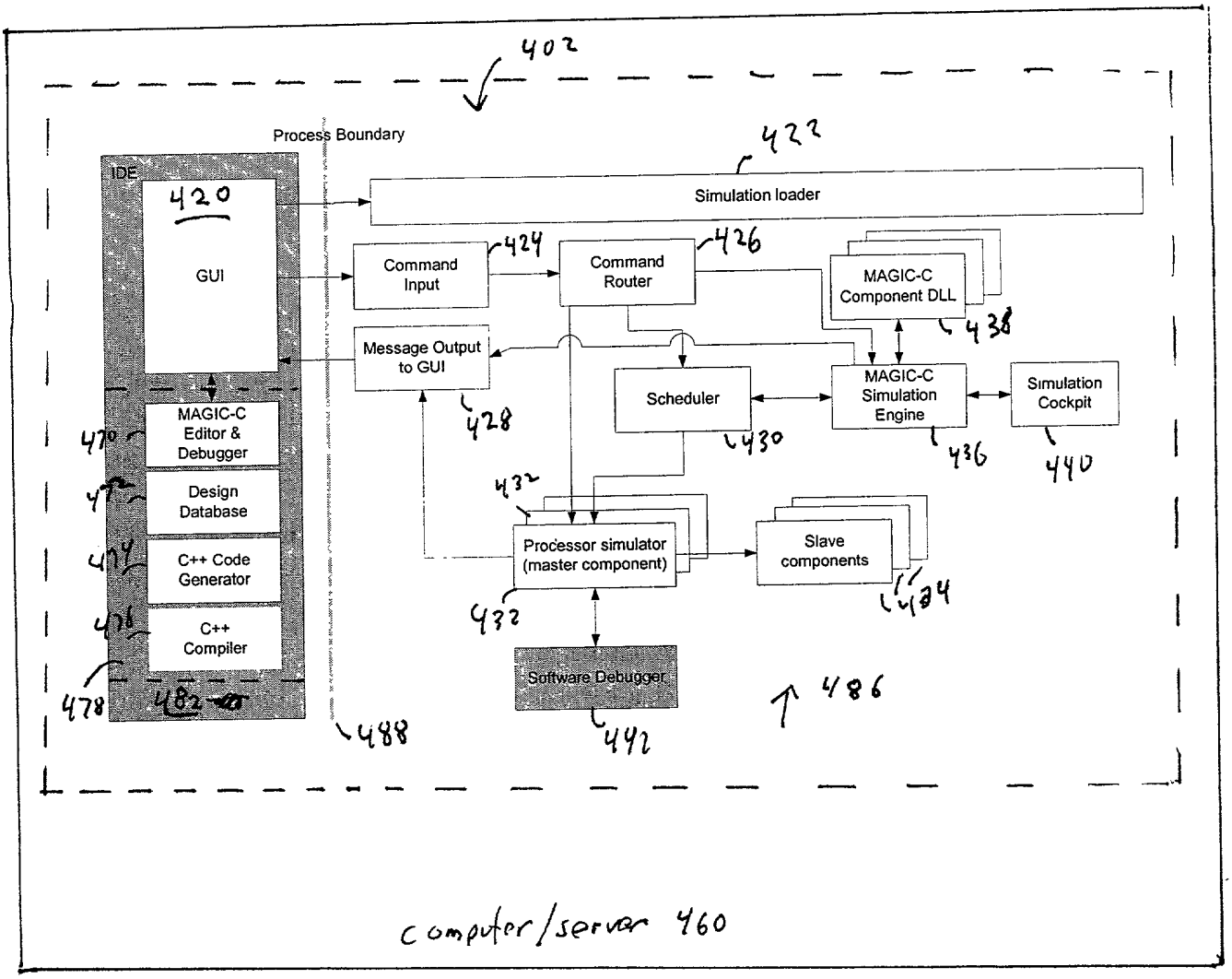

402
Process Boundary
IDE
420
GUI
422
Simulation loader
424
Command Input
426
Command Router
MAGIC-C Component DLL
438
Message Output to GUI
428
Scheduler
430
MAGIC-C Simulation Engine
436
Simulation Cockpit
440
470
MAGIC-C Editor & Debugger
472
Design Database
474
C++ Code Generator
476
C++ Compiler
478
482
488
432
Processor simulator (master component)
Slave components
434
Software Debugger
442
486
computer/server 460

FIG. 4A

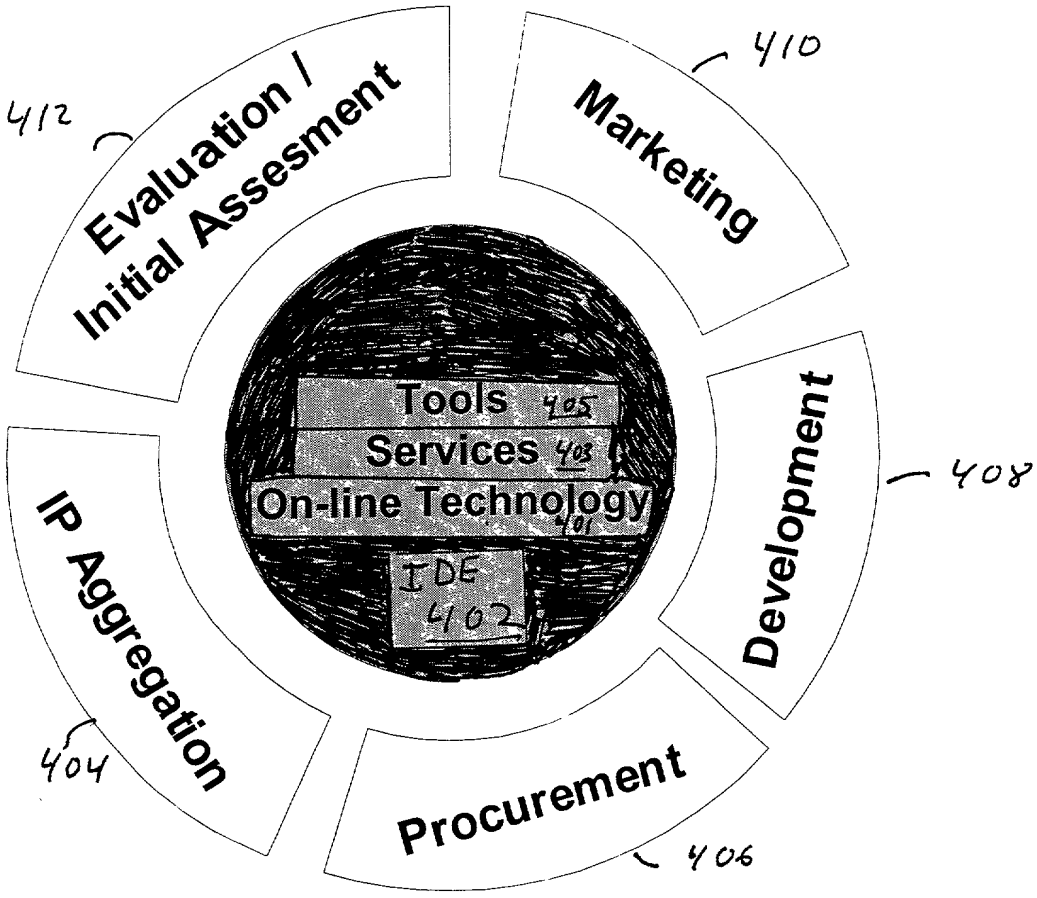

Evaluation / Initial Assesment
412
Marketing
410
Development
408
Procurement
406
IP Aggregation
404
Tools 405
Services 403
On-line Technology 401
IDE 402

FIG. 4B

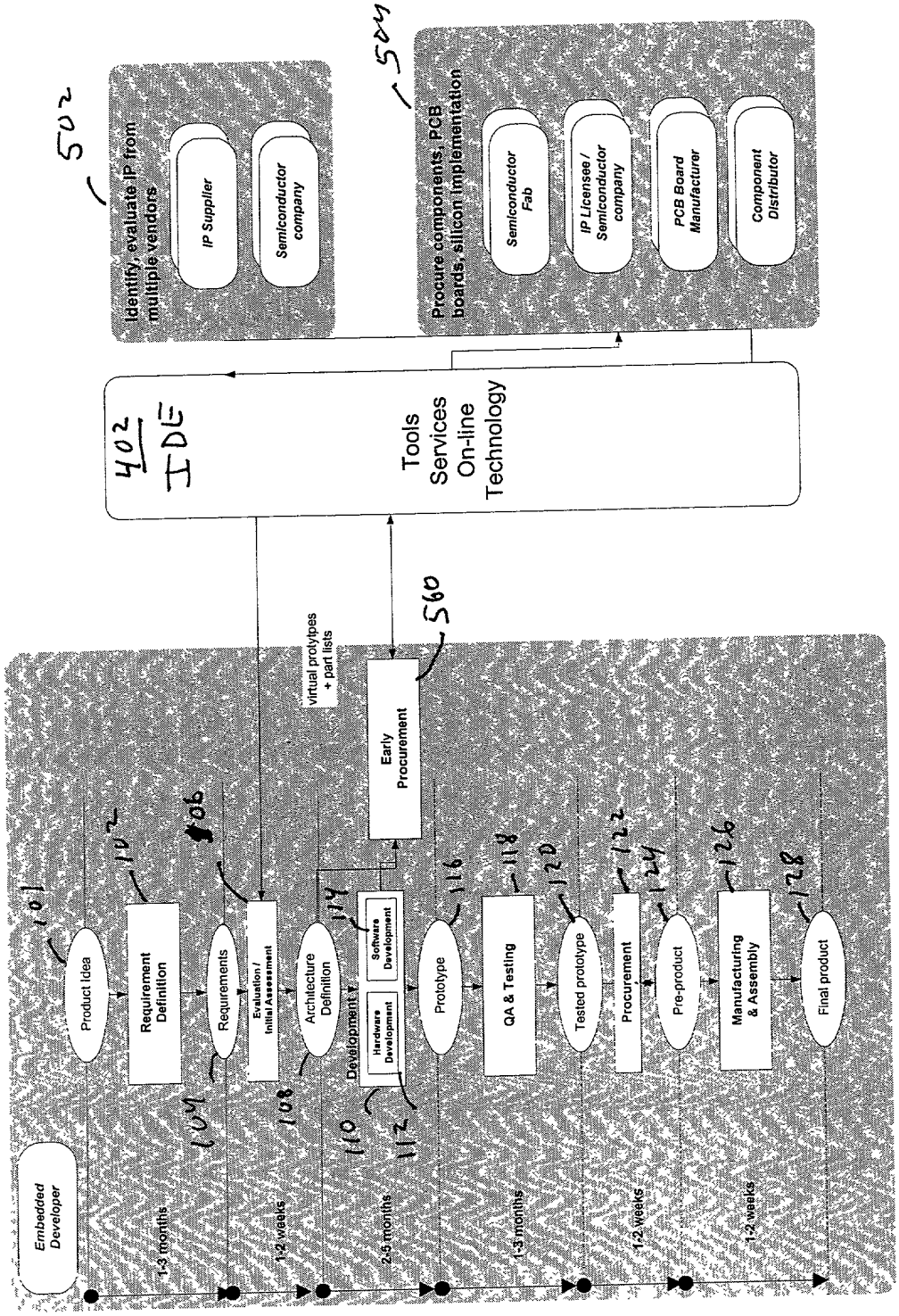

502
Identify, evaluate IP from multiple vendors
IP Supplier
Semiconductor company
504
Procure components, PCB boards, silicon implementation
Semiconductor Fab
IP Licensee / Semiconductor company
PCB Board Manufacturer
Component Distributor
402
IDE
Tools
Services
On-line
Technology
560
virtual prototypes + part lists
Early Procurement
Embedded Developer
Product Idea
Requirement Definition
Requirements
Evaluation / Initial Assessment
Architecture Definition
Development
Hardware Development
Software Development
Prototype
QA & Testing
Tested prototype
Procurement
Pre-product
Manufacturing & Assembly
Final product
1-3 months
1-2 weeks
2-5 months
1-3 months
1-2 weeks
1-2 weeks
101
102
104
106
108
110
112
114
116
118
120
122
124
126
128

FIG. 5

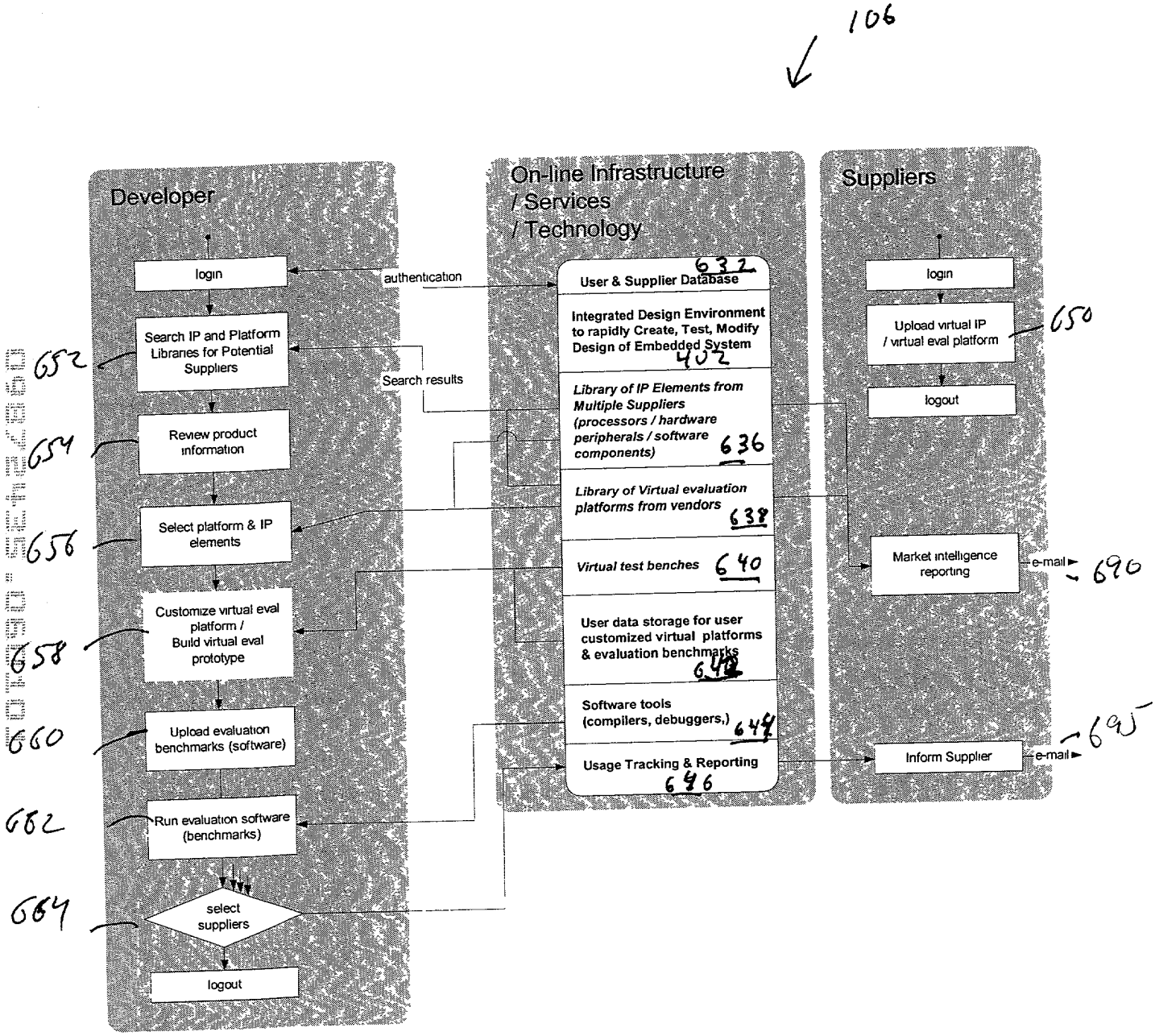

106
Developer
On-line Infrastructure / Services / Technology
Suppliers
login
authentication
User & Supplier Database 632
Integrated Design Environment to rapidly Create, Test, Modify Design of Embedded System 402
Library of IP Elements from Multiple Suppliers (processors / hardware peripherals / software components) 636
Library of Virtual evaluation platforms from vendors 638
Virtual test benches 640
User data storage for user customized virtual platforms & evaluation benchmarks 642
Software tools (compilers, debuggers,) 644
Usage Tracking & Reporting 646
Search IP and Platform Libraries for Potential Suppliers 652
Search results
Review product information 654
Select platform & IP elements 656
Customize virtual eval platform / Build virtual eval prototype 658
Upload evaluation benchmarks (software) 660
Run evaluation software (benchmarks) 662
select suppliers 664
logout
login
Upload virtual IP / virtual eval platform 650
logout
Market intelligence reporting
e-mail 690
Inform Supplier
e-mail 695

FIG. 6

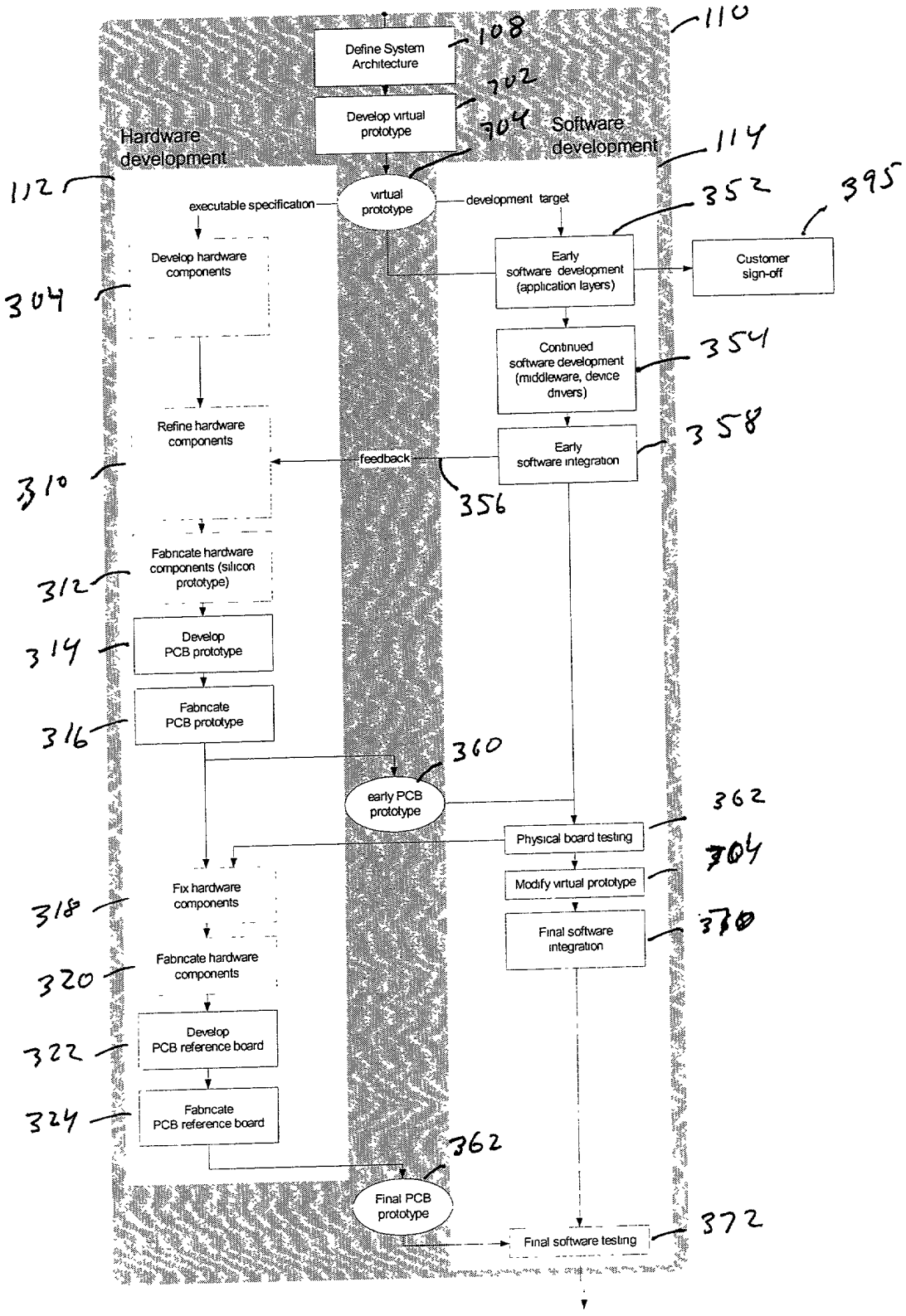

Define System Architecture
108
110
Develop virtual prototype
202
Hardware development
Software development
114
112
virtual prototype
executable specification
development target
352
395
Develop hardware components
304
Early software development (application layers)
Customer sign-off
Continued software development (middleware, device drivers)
354
Refine hardware components
Early software integration
358
feedback
310
356
Fabricate hardware components (silicon prototype)
312
Develop PCB prototype
314
Fabricate PCB prototype
316
360
early PCB prototype
362
Physical board testing
304
Modify virtual prototype
Fix hardware components
318
Final software integration
370
Fabricate hardware components
320
Develop PCB reference board
322
Fabricate PCB reference board
324
362
Final PCB prototype
Final software testing
372

FIG. 7

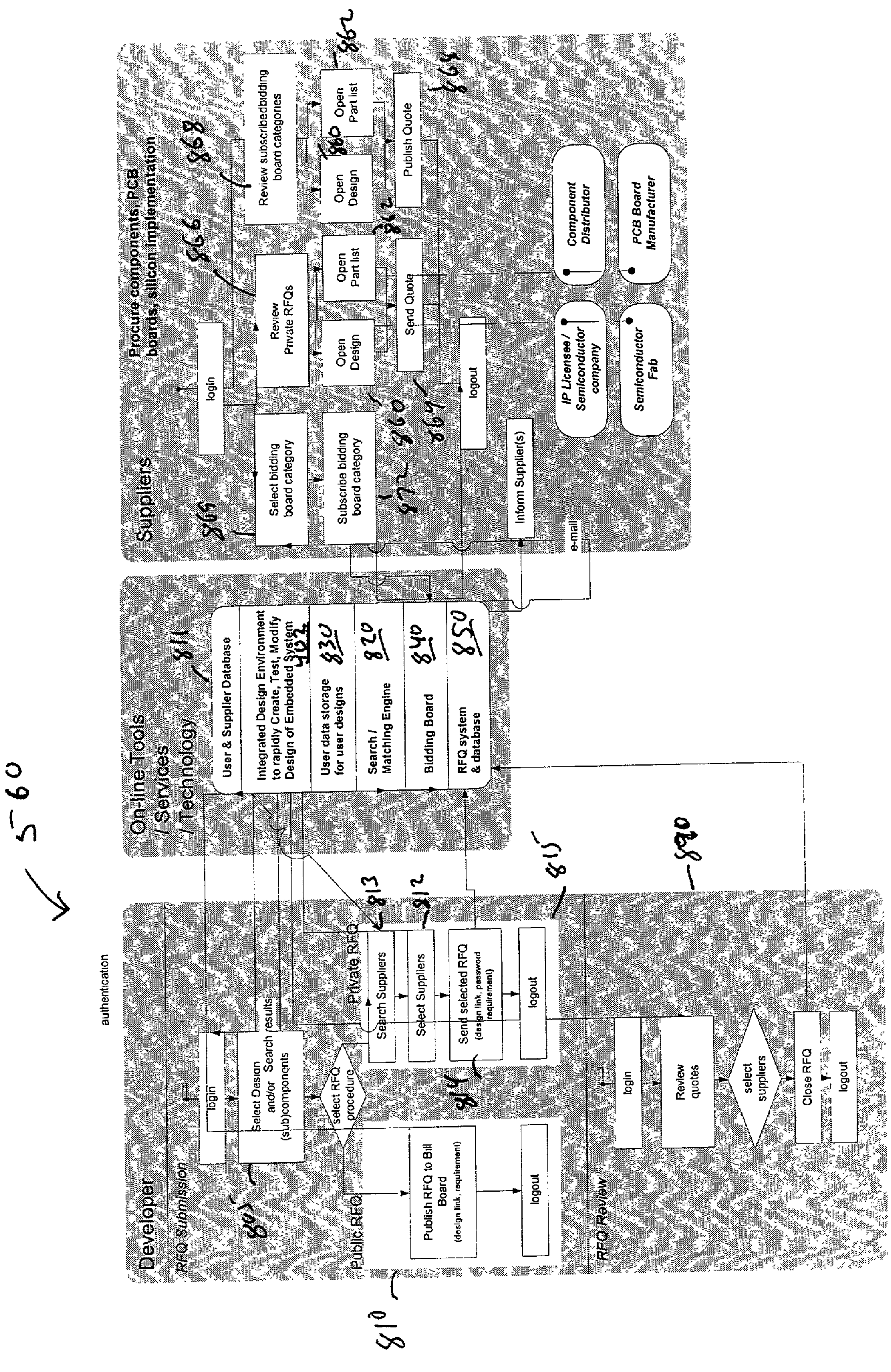

560
Developer
RFQ Submission
authentication
login
Select Design and/or (sub)components
Search results
select RFQ procedure
Public RFQ
Publish RFQ to Bill Board (design link, requirement)
logout
Private RFQ
Search Suppliers
Select Suppliers
Send selected RFQ (design link, password requirement)
logout
RFQ Review
login
Review quotes
select suppliers
Close RFQ
logout
805
810
812
813
814
815
890
On-line Tools / Services / Technology
811
User & Supplier Database
Integrated Design Environment to rapidly Create, Test, Modify Design of Embedded System
402
User data storage for user designs
830
Search / Matching Engine
820
Bidding Board
840
RFQ system & database
850
Suppliers
Procure components, PCB boards, silicon implementation
login
Select bidding board category
Subscribe bidding board category
Review Private RFQs
Open Design
Open Part list
Send Quote
logout
Review subscribedbidding board categories
Open Design
Open Part list
Publish Quote
Inform Supplier(s)
e-mail
IP Licensee / Semiconductor company
Semiconductor Fab
Component Distributor
PCB Board Manufacturer
865
866
868
860
862
864
872

FIG. 8

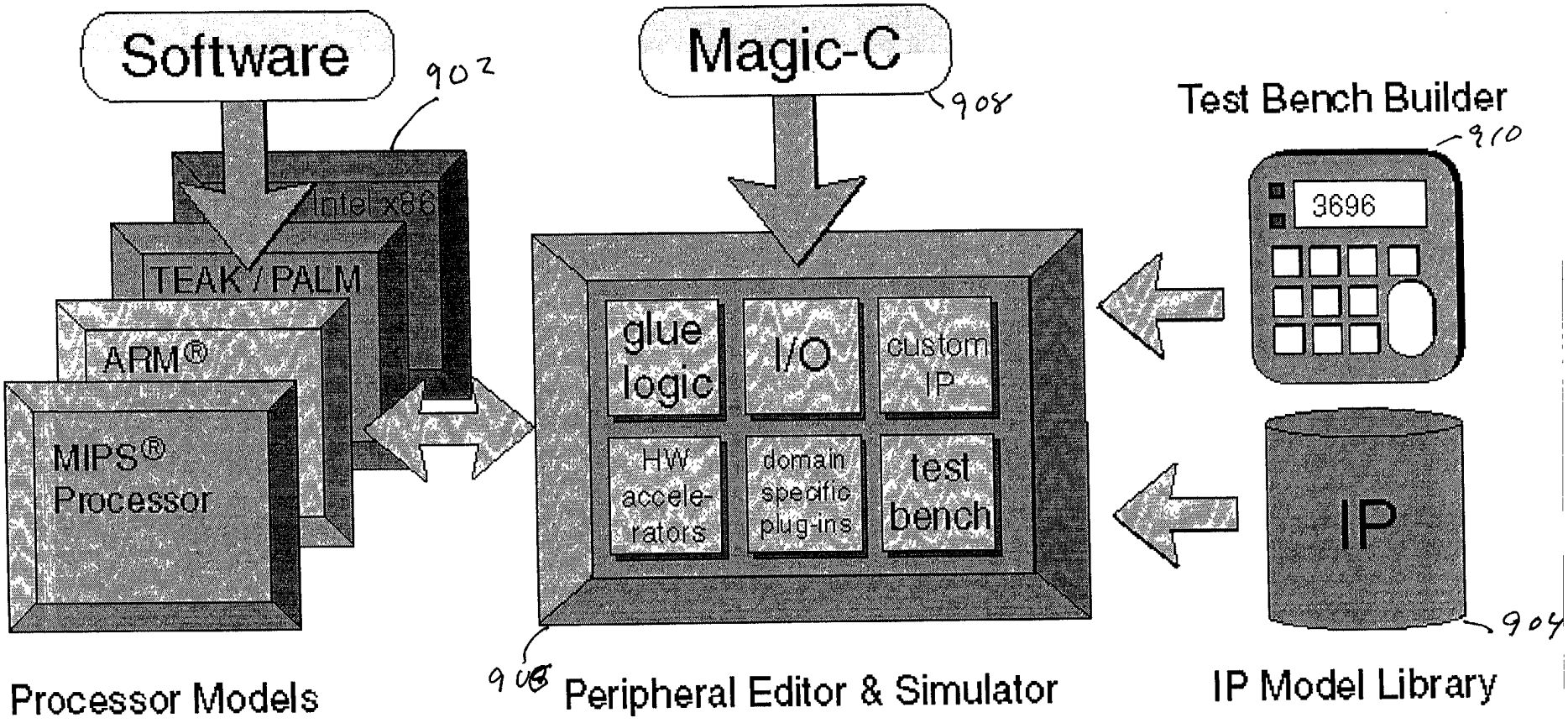

Software
902
Magic-C
908
Test Bench Builder
910
Intel x86
TEAK / PALM
ARM®
MIPS®
Processor
glue logic
I/O
custom IP
HW accele-rators
domain specific plug-ins
test bench
3696
IP
904
Processor Models
908
Peripheral Editor & Simulator
IP Model Library

FIG. 9

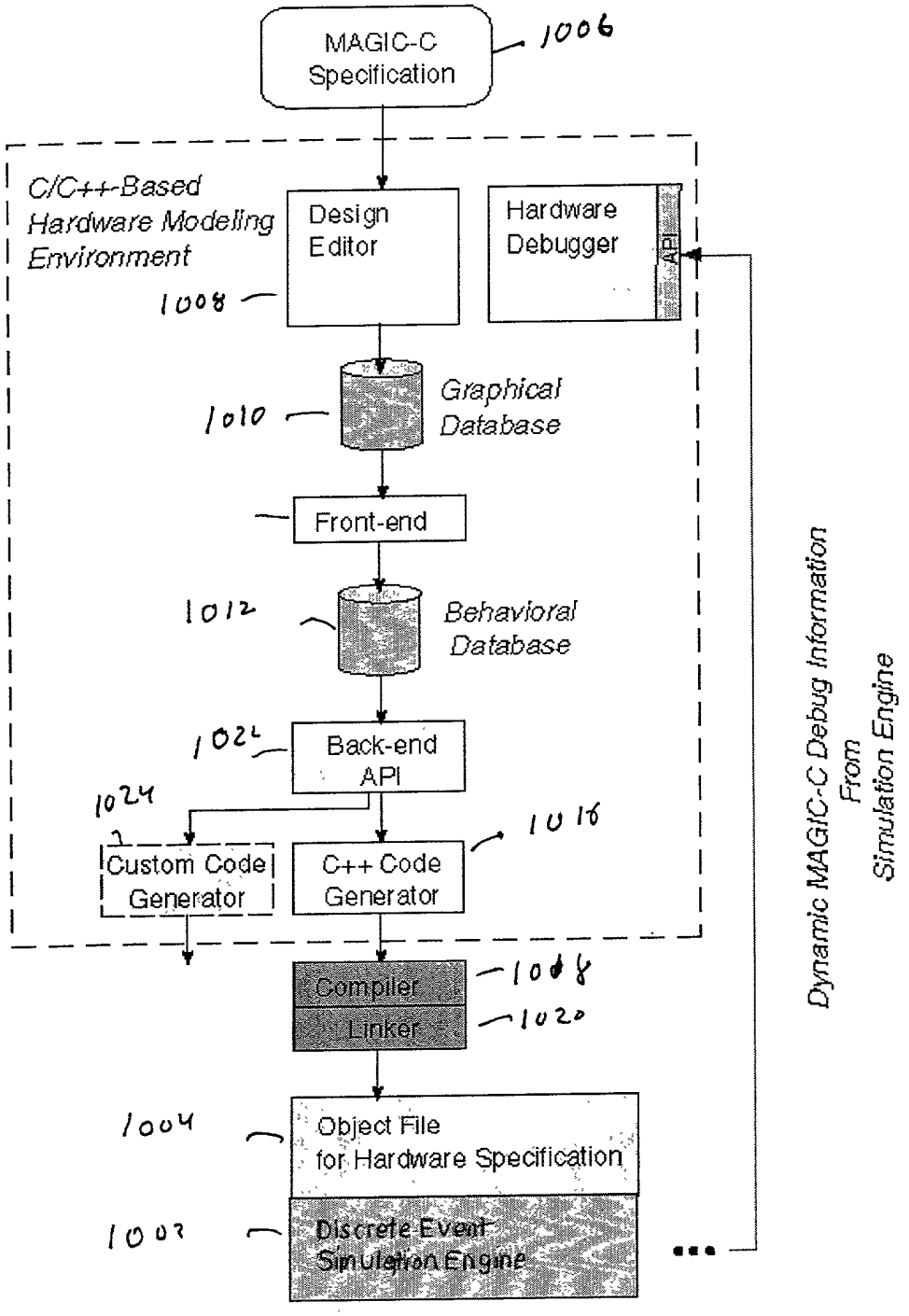

MAGIC-C Specification
1006
C/C++-Based Hardware Modeling Environment
Design Editor
1008
Hardware Debugger
API
Graphical Database
1010
Front-end
Behavioral Database
1012
Back-end API
1024
1014
Custom Code Generator
C++ Code Generator
1016
Compiler
1018
Linker
1020
Object File for Hardware Specification
1004
Discrete Event Simulation Engine
1002
Dynamic MAGIC-C Debug Information From Simulation Engine

FIG. 10

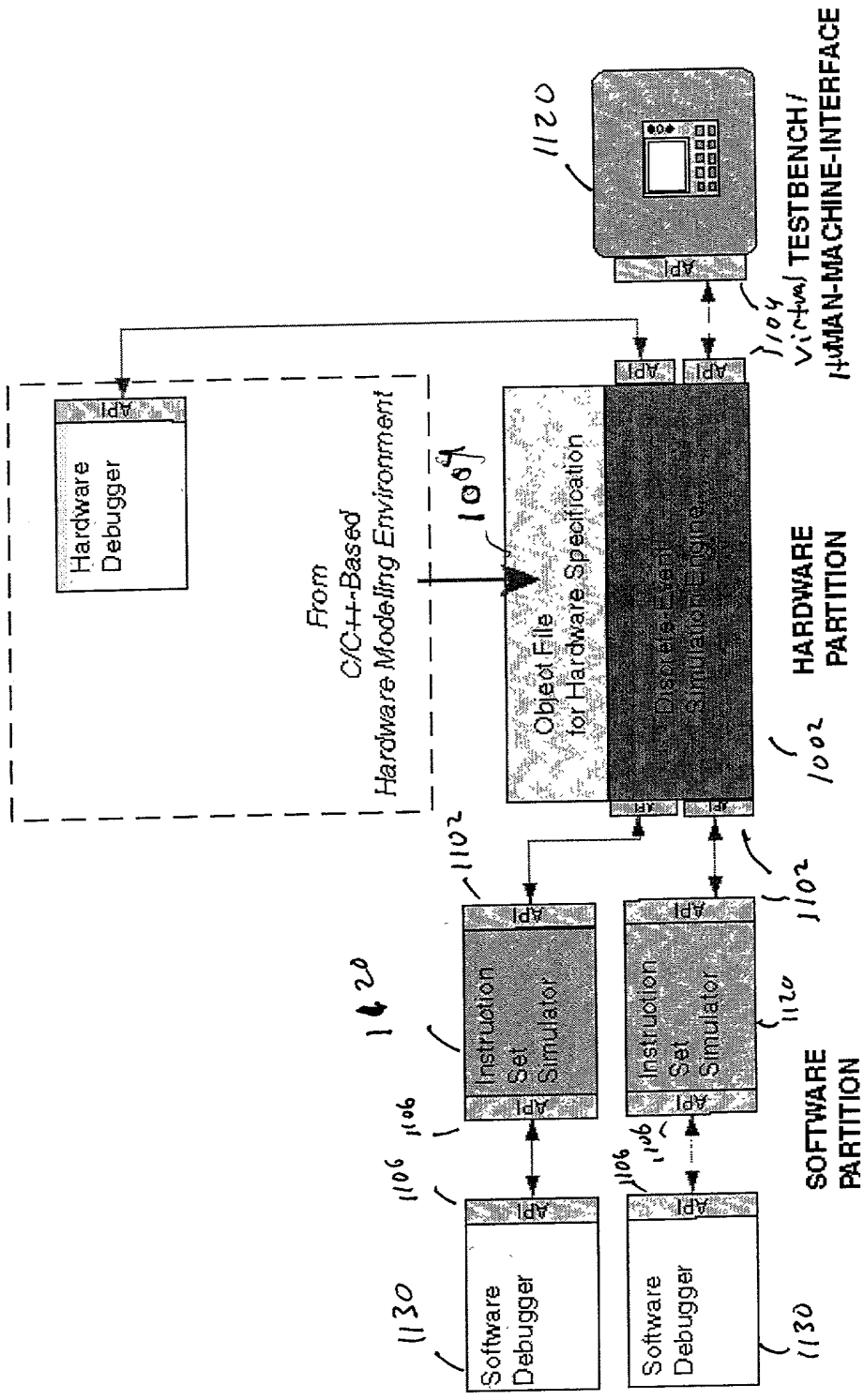

1120
API
1104
Virtual TESTBENCH/
HUMAN-MACHINE-INTERFACE
Hardware
Debugger
From
C/C++-Based
Hardware Modelling Environment
1004
Object File
for Hardware Specification
Discrete-Event
Simulator Engine
HARDWARE
PARTITION
1002
1102
1102
1120
Instruction
Set
Simulator
Instruction
Set
Simulator
SOFTWARE
PARTITION
1106
1106
1106
1106
Software
Debugger
Software
Debugger
1130
1130

FIG. 11

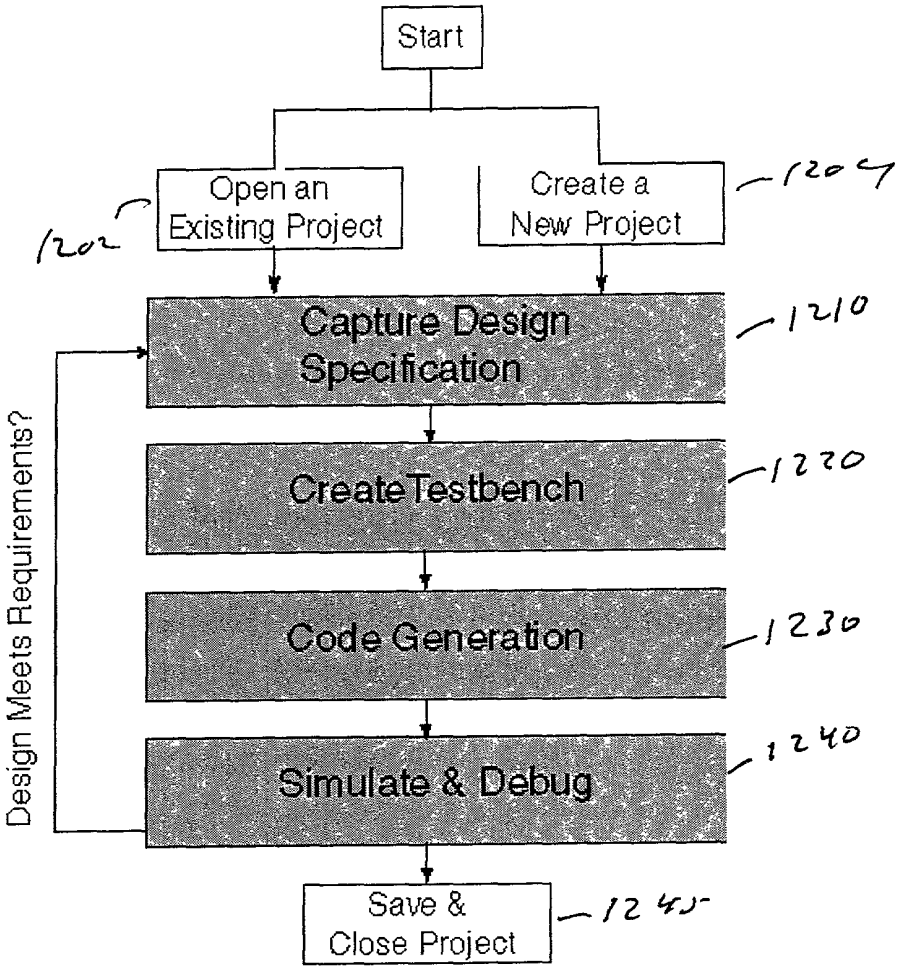

1200
Start
Open an Existing Project
1202
Create a New Project
1204
Capture Design Specification
1210
CreateTestbench
1220
Code Generation
1230
Simulate & Debug
1240
Design Meets Requirements?
Save & Close Project
1245

FIG. 12

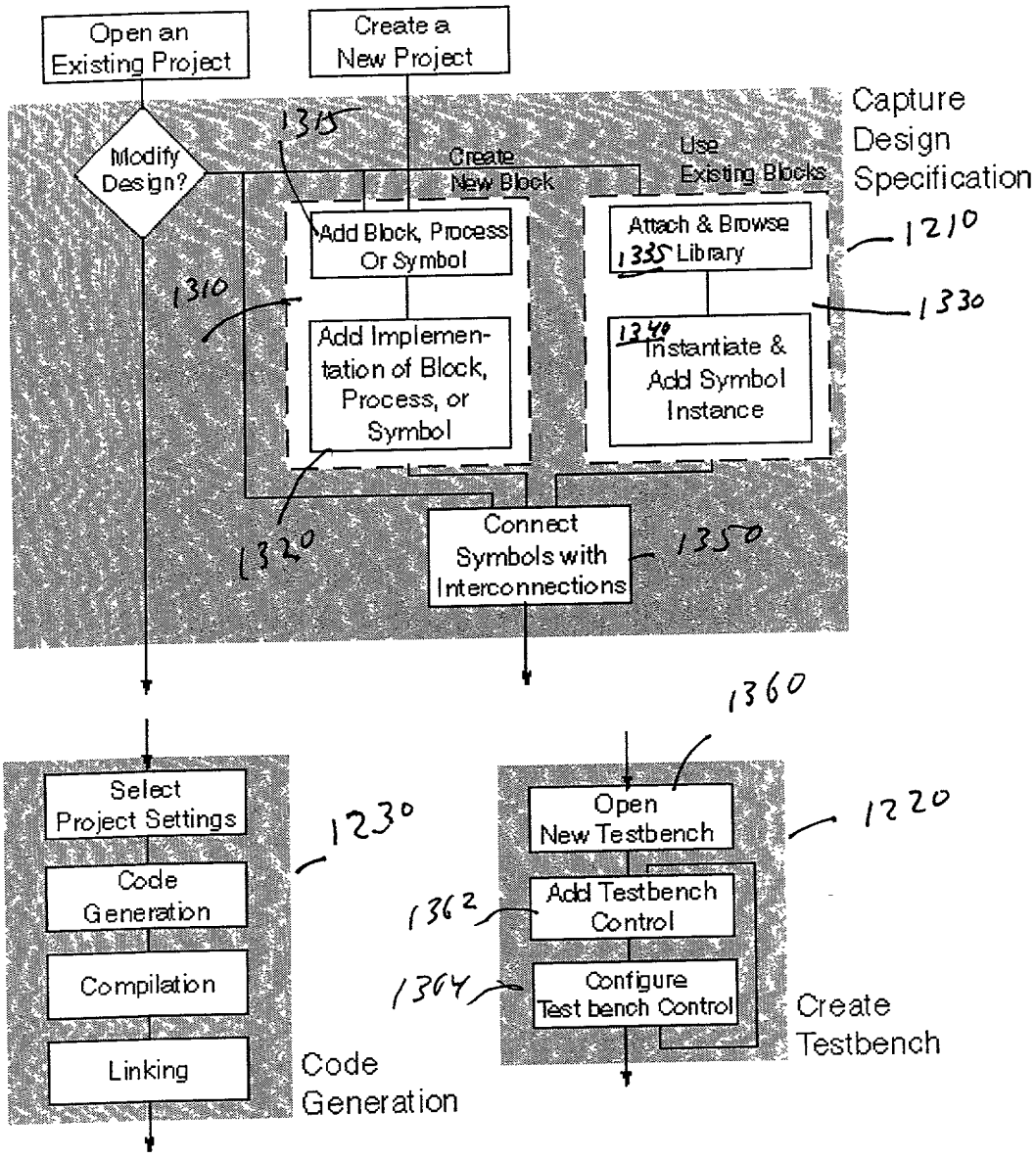

Open an Existing Project
Create a New Project
Modify Design?
1305
Create New Block
Use Existing Blocks
Add Block, Process Or Symbol
Attach & Browse 1335 Library
1210
1310
Add Implementation of Block, Process, or Symbol
1340 Instantiate & Add Symbol Instance
1330
Capture Design Specification
1320
Connect Symbols with Interconnections
1350
1360
Select Project Settings
1230
Code Generation
Compilation
Linking
Code Generation
Open New Testbench
1220
1362
Add Testbench Control
1364
Configure Test bench Control
Create Testbench

FIG. 13

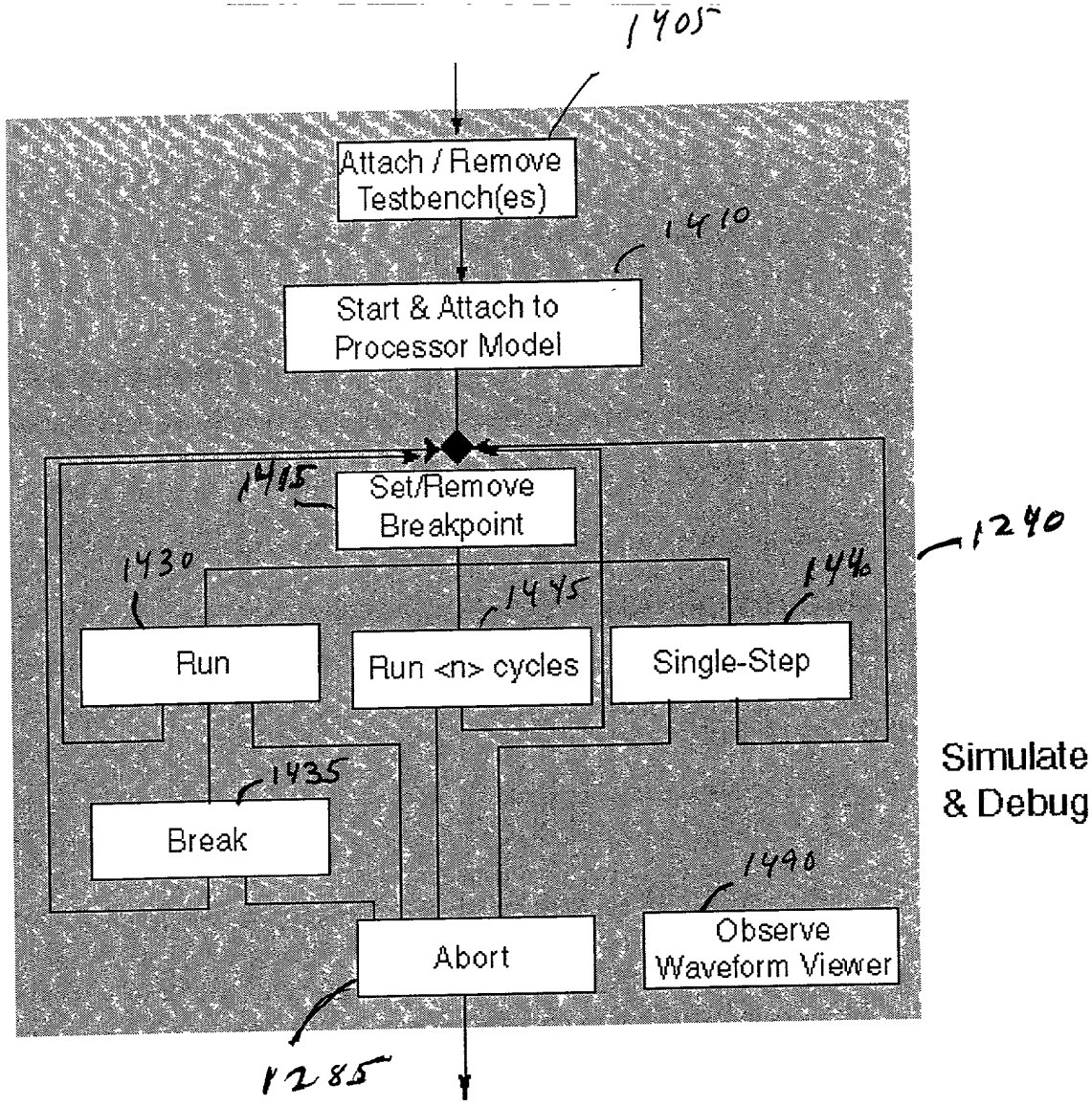

1405
Attach / Remove Testbench(es)
1410
Start & Attach to Processor Model
1415
Set/Remove Breakpoint
1420
Run
1425
Run <n> cycles
1440
Single-Step
1435
Break
1490
Observe Waveform Viewer
Abort
1285
1240
Simulate & Debug

FIG. 14

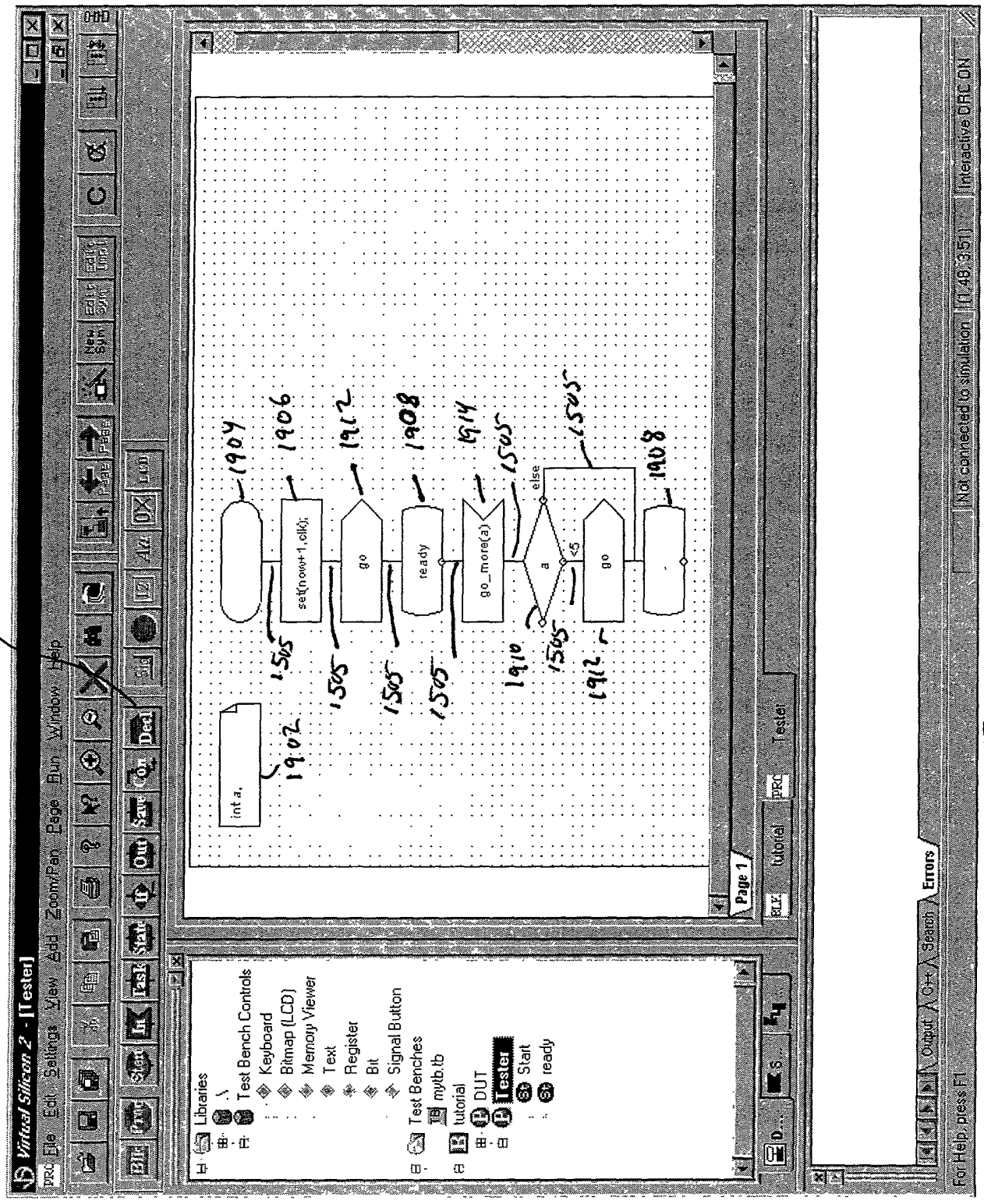

Virtual Silicon 2 - [Tester]
File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
Test Bench Controls
Keyboard
Bitmap (LCD)
Memory Viewer
Text
Register
Bit
Signal Button
Test Benches
mytb.tb
tutorial
DUT
Tester
Start
ready
int a;
setKnown=1,clk);
go
ready
go_more(a)
a
else
<5
go
Page 1
Tutorial
Tester
Output
C++
Search
Errors
For Help, press F1
Not connected to simulation
Interactive DRC ON

FIG. 15

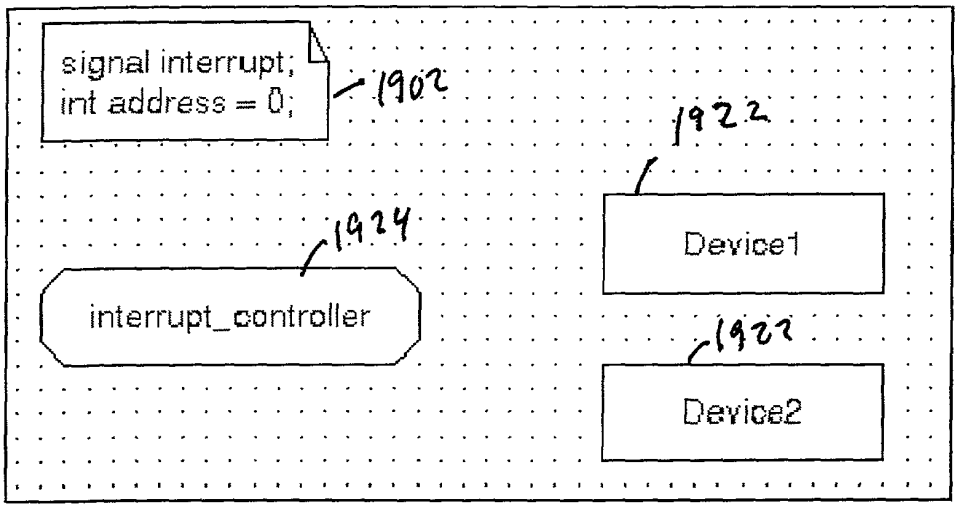


FIG. 16

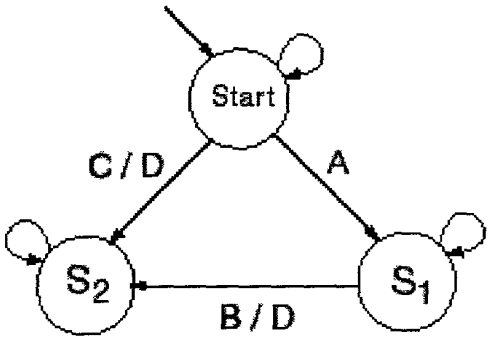


FIG. 17a)

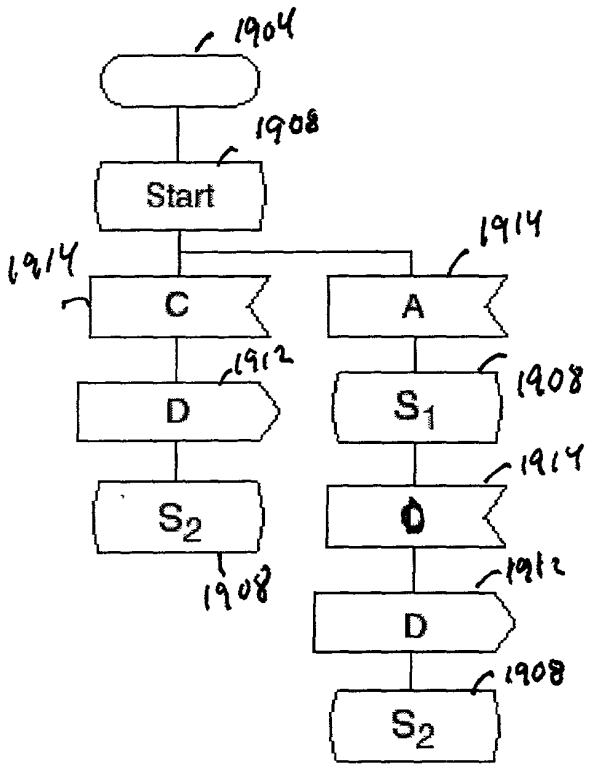


FIG. 17 (b)

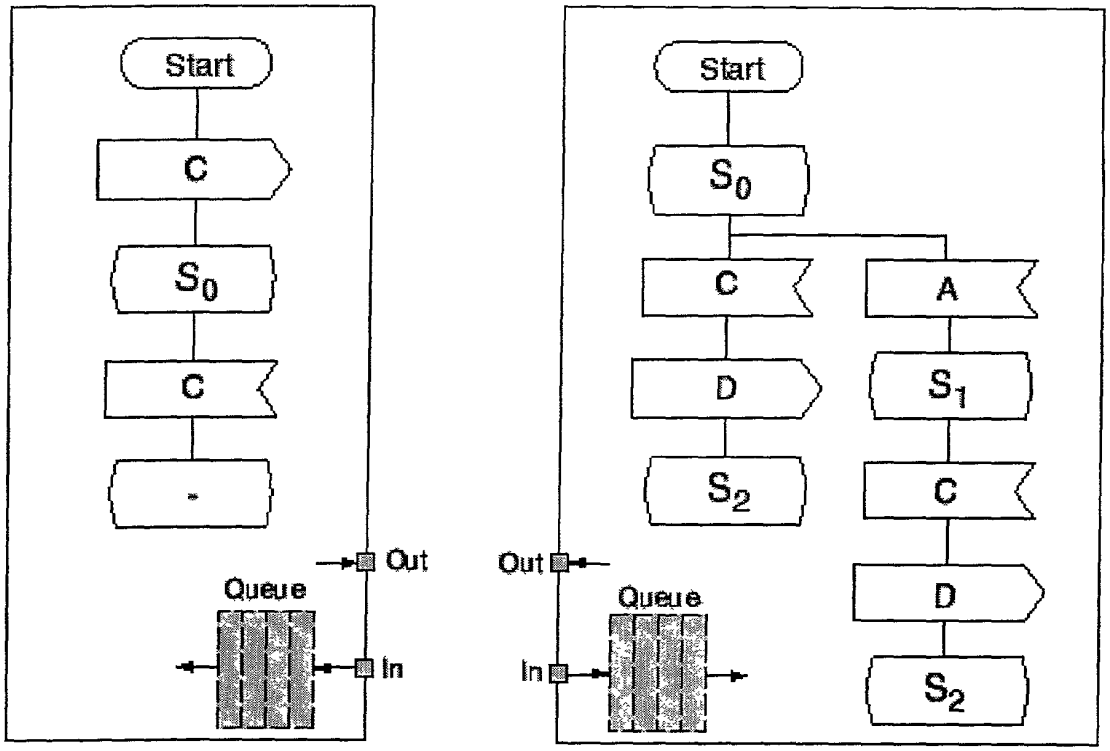


FIG. 18

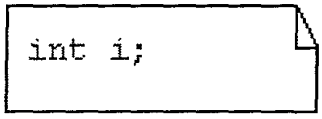
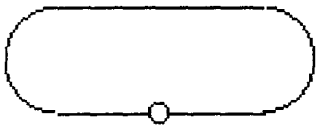
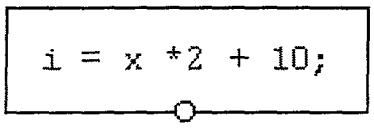
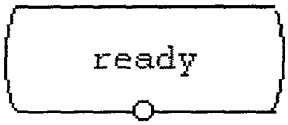
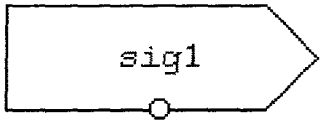
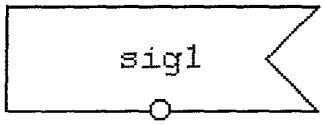
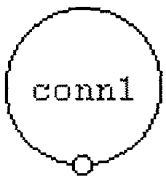
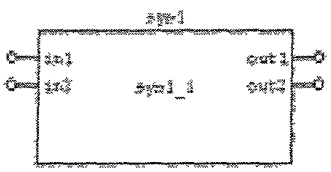
Name	Graphical symbol	Description
Declaration		defines local variables and signals.
Start		Starting point of the Finite State Machine execution at initialization time.
Task		Execution block, containing ANSI-C statements to be executed.
State		Location where FSM waits in until a triggering Signal is received.
Decision		Directs execution flow based on the result of expression evaluation inside the decision construct.
Signal-Out		Sending of a communication signal (with an optional payload).
Signal-In		Receiving of a communication signal (with an optional payload)
Connector		Allows to split designs over multiple pages, and connects the control flow between these different pages.

FIG 19A

Symbol		Captures design hierarchy and structure. Communication is done through pins on the outline of the symbol. Allows to re-use functional behavior by supporting multiple instances.
Blocks		Captures design hierarchy and structure. Communication is done through signals declared at higher scopes. Communication is done by signal name matching (rather than by pin connection). A block can contain multiple processes.
Process		Acts as leaf node in the design hierarchy, and captures a single FSM. By definition, all processes are concurrent at all times.

1920
1922
1924

FIG. 19B

```
// External interface
extern_signal WR(unsigned int,unsigned int, unsigned int);
extern_signal RD(unsigned int,unsigned int);
extern_signal Write_Ack;
extern_signal Read_Data(unsigned int);
extern_signal CNTINTR(unsigned int);
// Local variables
signal start_clk;
clock clk;
bool clock_started;
unsigned int LIMIT; //write register
VS_int COUNT;
//temp vars
unsigned int data,width, addr;
```

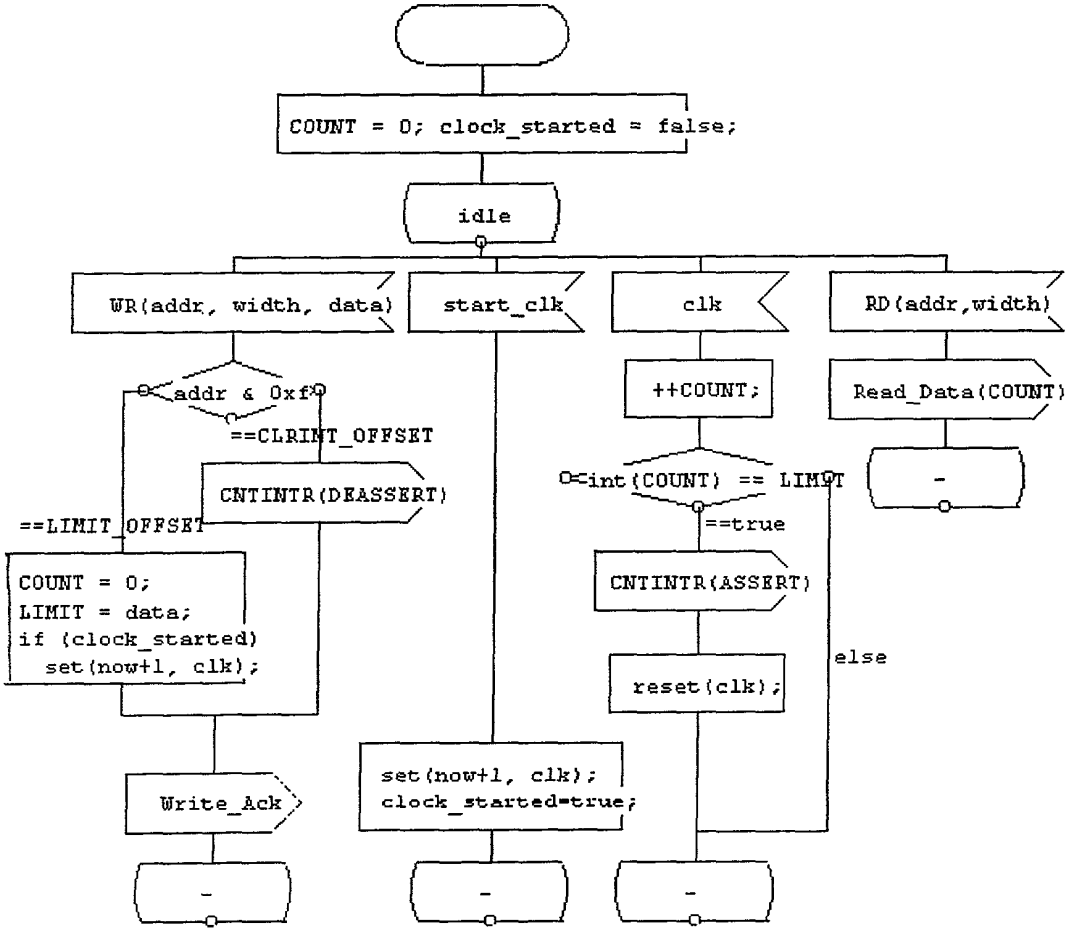


FIG. 20

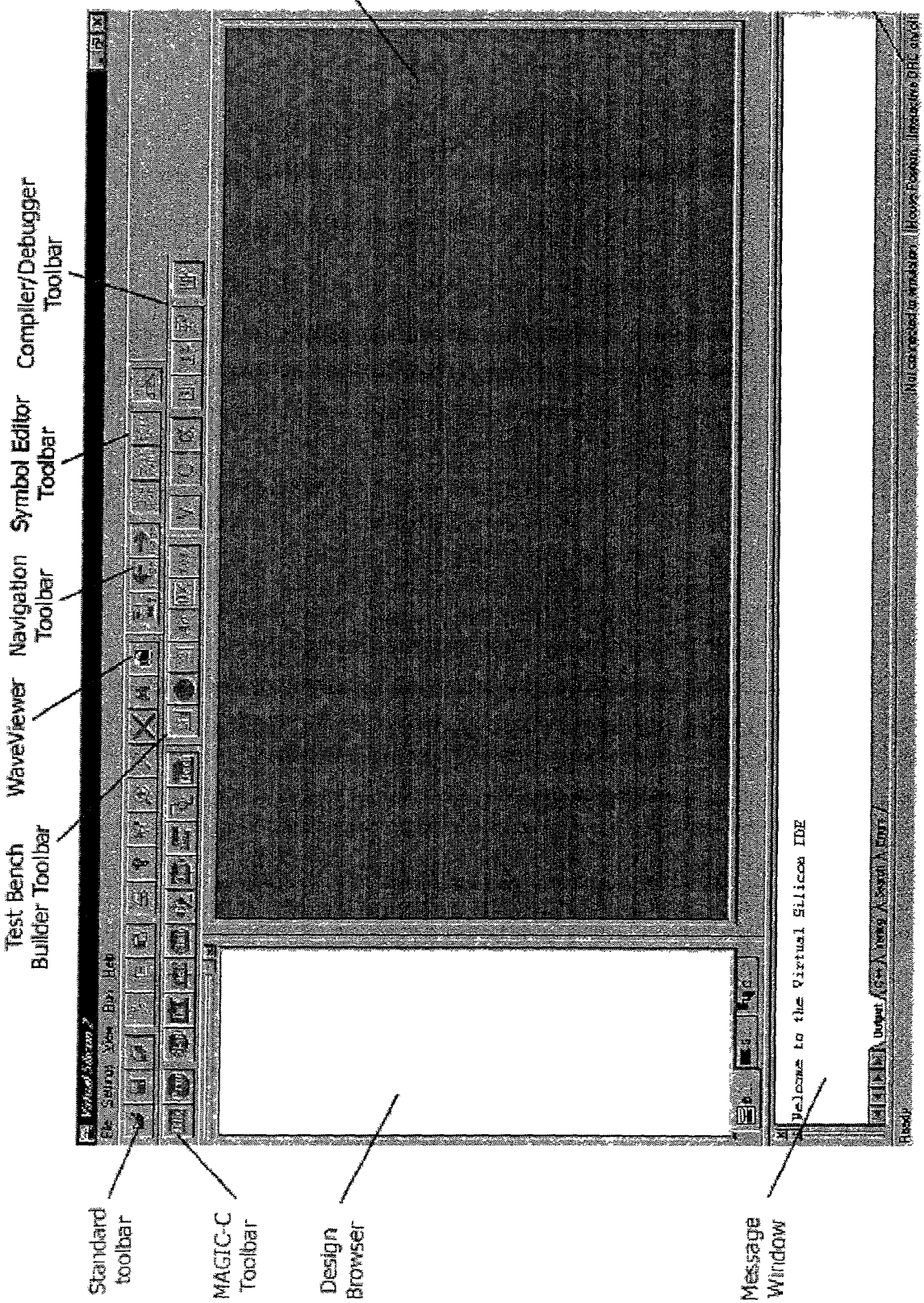

Design Window
Compiler/Debugger Toolbar
Symbol Editor Toolbar
Navigation Toolbar
WaveViewer
Test Bench Builder Toolbar
Standard toolbar
MAGIC-C Toolbar
Design Browser
Message Window
Welcome to the Virtual Silicon IDE

FIG. 21

FIG. 22

Standard Toolbar

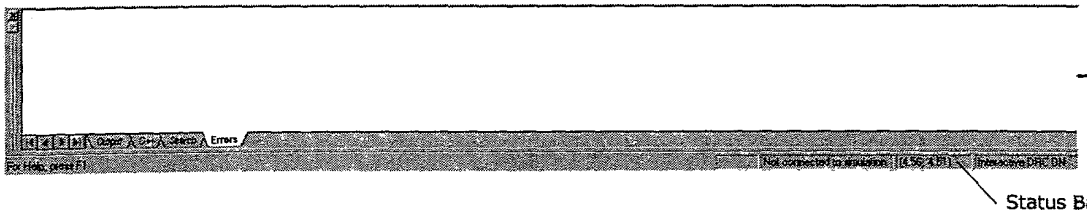


FIG 23

Message Window, Showing Different Message Tabs, and the Status Bar

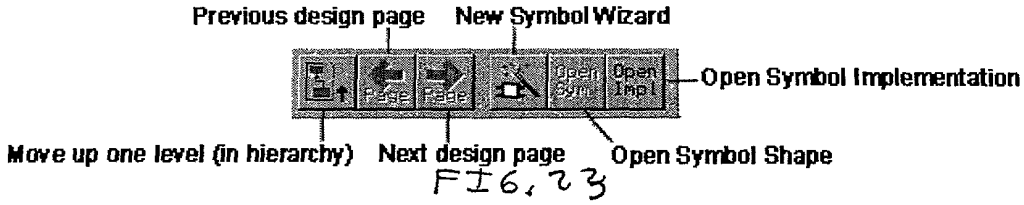


FIG. 23

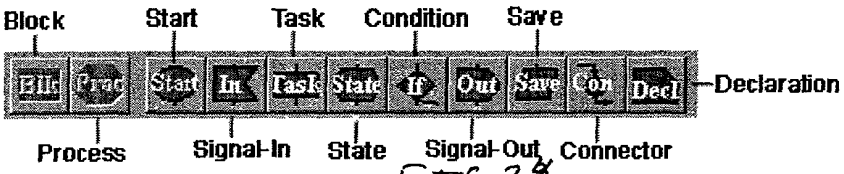


FIG. 24

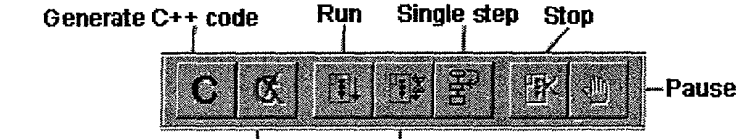


FIG. 25

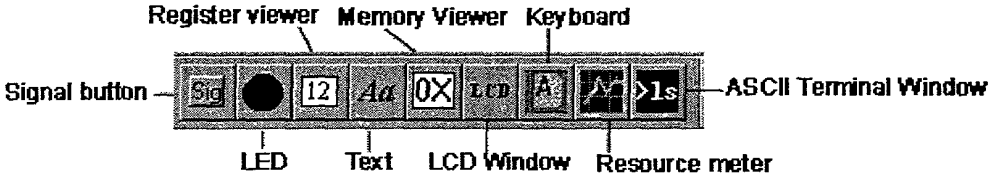


FIG. 26

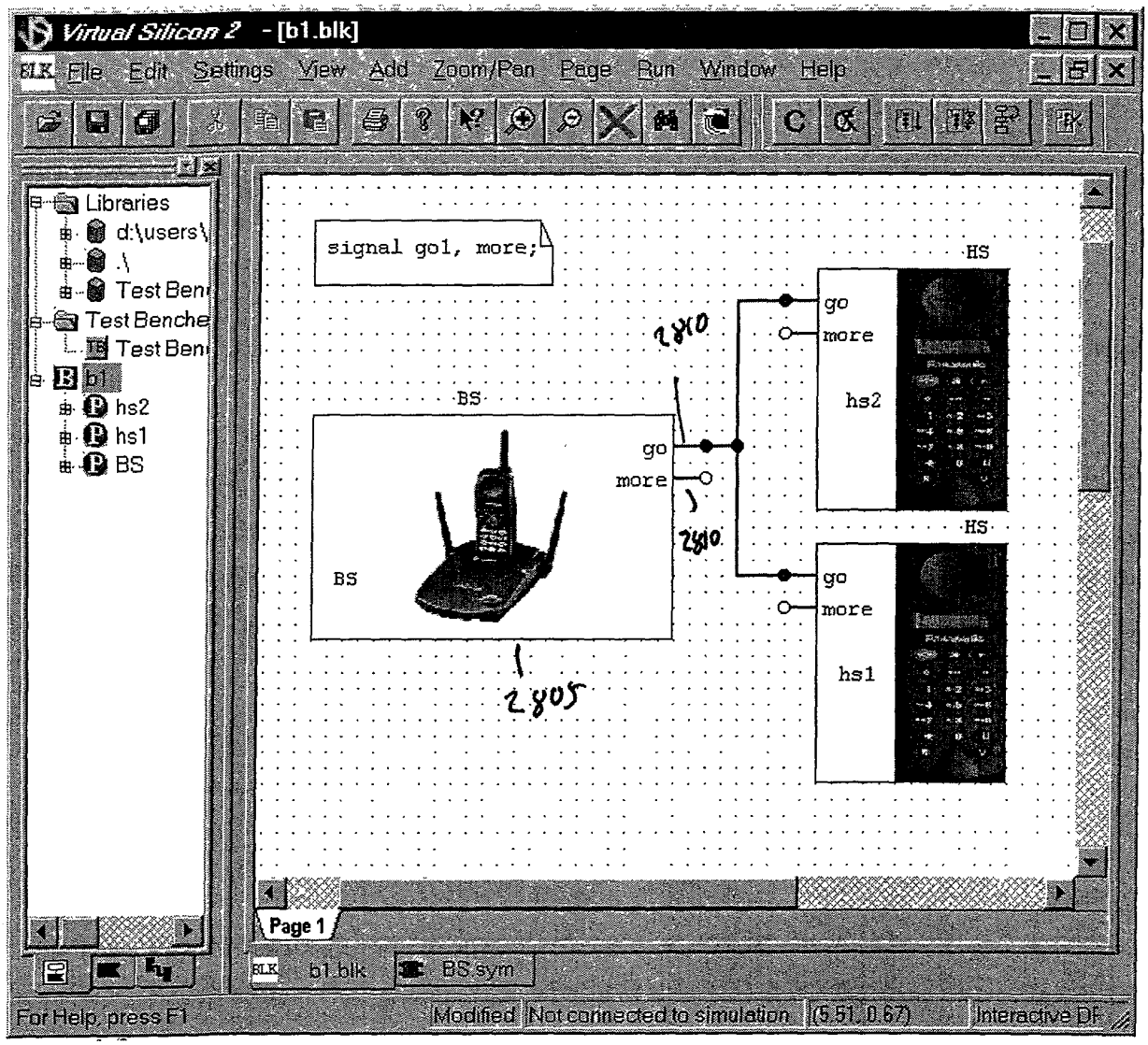

Virtual Silicon 2 - [b1.blk]
File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
d:\users\
.\
Test Ben
Test Benche
Test Ben
b1
hs2
hs1
BS
signal go1, more;
HS
go
more
hs2
2810
BS
go
more
2810
HS
go
more
hs1
BS
2805
Page 1
b1.blk
BS sym
For Help, press F1
Modified
Not connected to simulation
(5.51, 0.67)
Interactive DF

FIG. 28

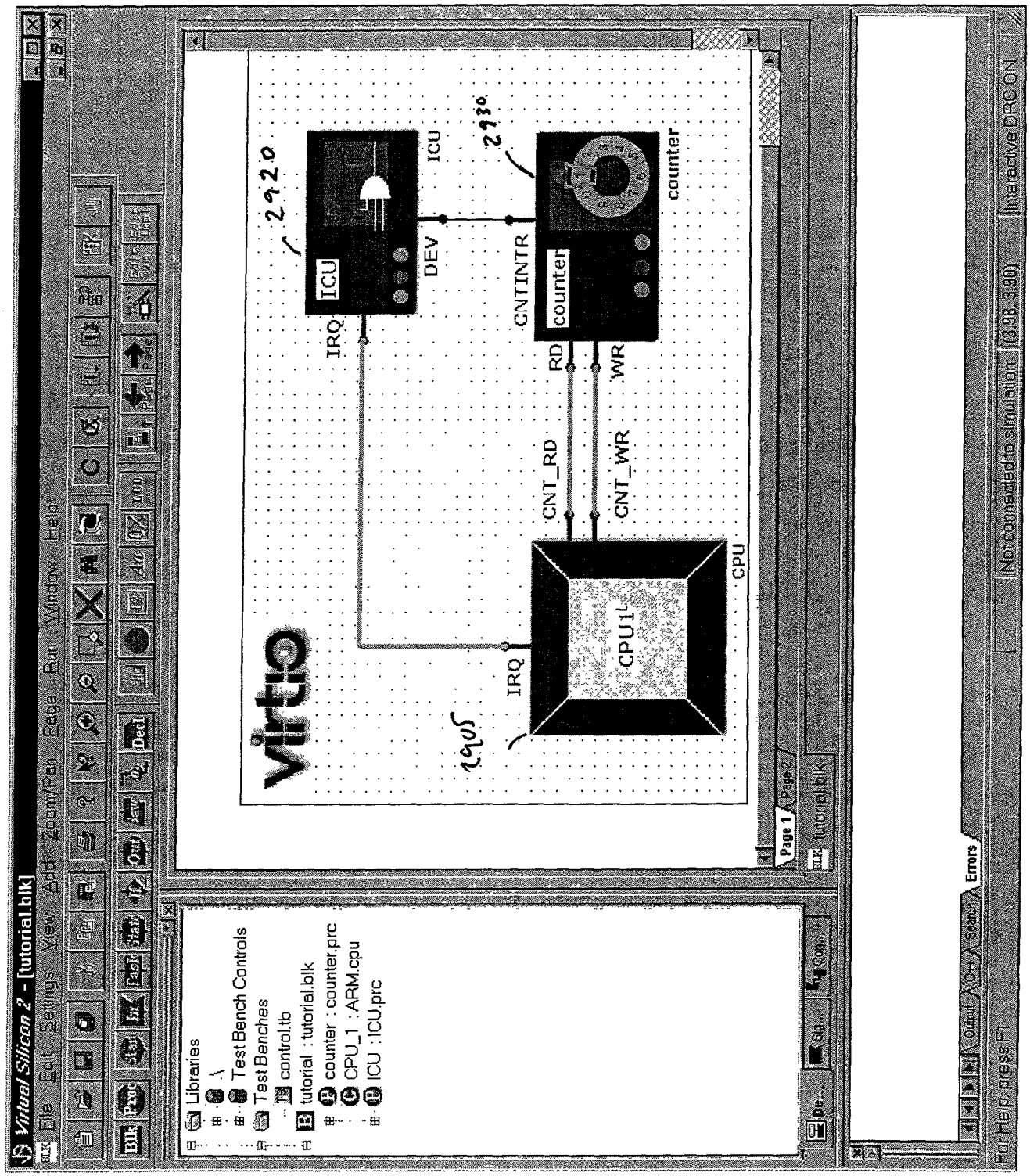

Virtual Silicon 2 - [tutorial.blk]
File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
Test Bench Controls
Test Benches
control.tb
tutorial : tutorial.blk
counter : counter.prc
CPU_1 : ARM.cpu
ICU : ICU.prc
virtio
2920
2930
2905
ICU
DEV
IRQ
CNTINTR
counter
RD
WR
CNT_RD
CNT_WR
CPU1
CPU
Page 1
Page 2
tutorial.blk
Output
C++
Search
Errors
For Help, press F1
Not connected to simulation
Interactive DRC ON

FIG. 29

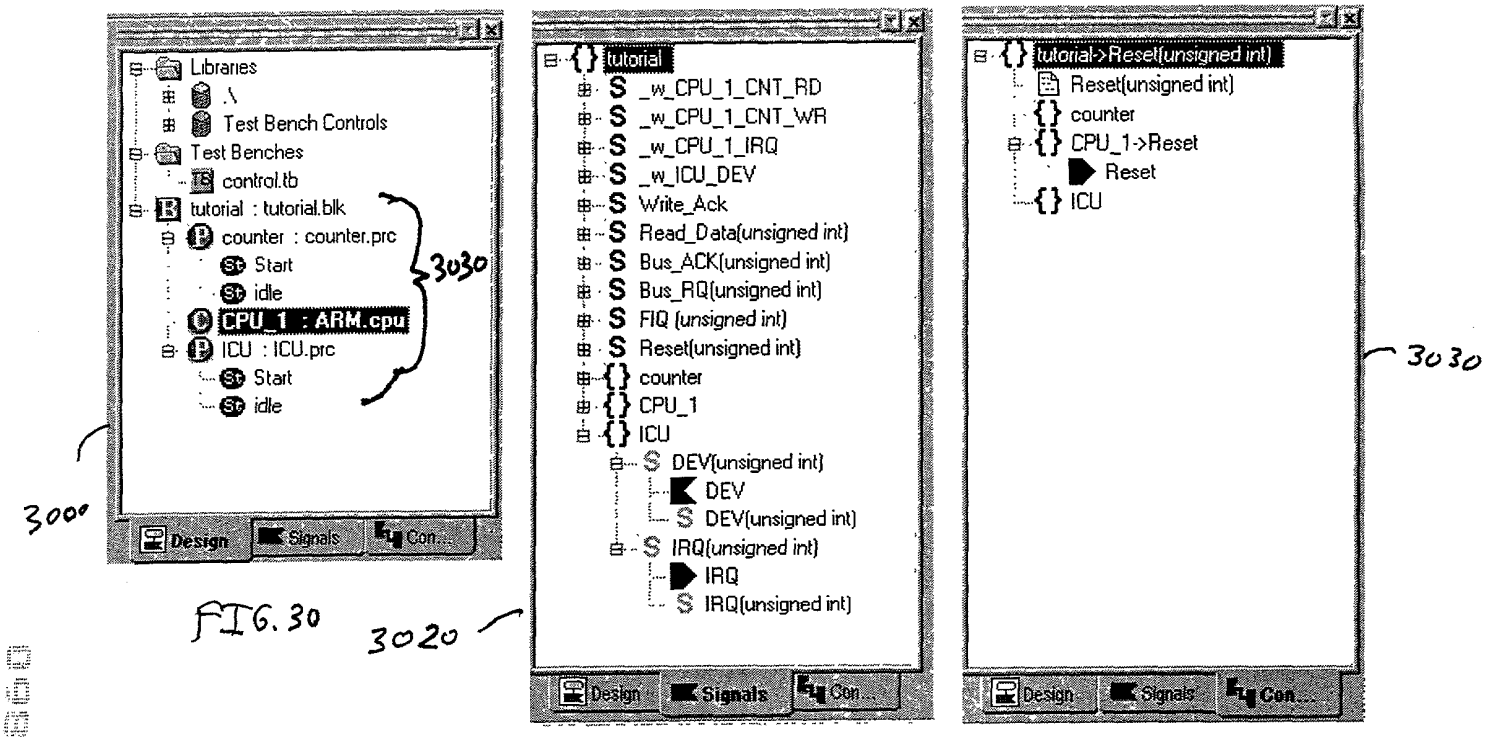

Libraries
.\
Test Bench Controls
Test Benches
control.tb
tutorial : tutorial.blk
counter : counter.prc
Start
idle
CPU_1 : ARM.cpu
ICU : ICU.prc
Start
idle
3030
3000
Design
Signals
Con...
tutorial
_w_CPU_1_CNT_RD
_w_CPU_1_CNT_WR
_w_CPU_1_IRQ
_w_ICU_DEV
Write_Ack
Read_Data(unsigned int)
Bus_ACK(unsigned int)
Bus_RQ(unsigned int)
FIQ (unsigned int)
Reset(unsigned int)
counter
CPU_1
ICU
DEV(unsigned int)
DEV
DEV(unsigned int)
IRQ(unsigned int)
IRQ
IRQ(unsigned int)
3020
tutorial->Reset(unsigned int)
Reset(unsigned int)
counter
CPU_1->Reset
Reset
ICU
3030

FIG. 30

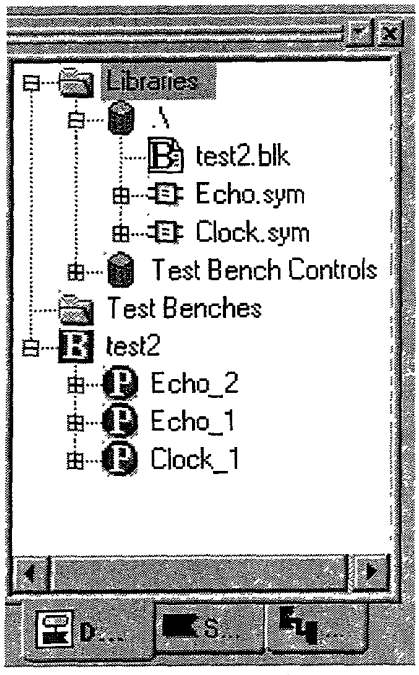

Libraries
.\
test2.blk
Echo.sym
Clock.sym
Test Bench Controls
Test Benches
test2
Echo_2
Echo_1
Clock_1

FIG. 31

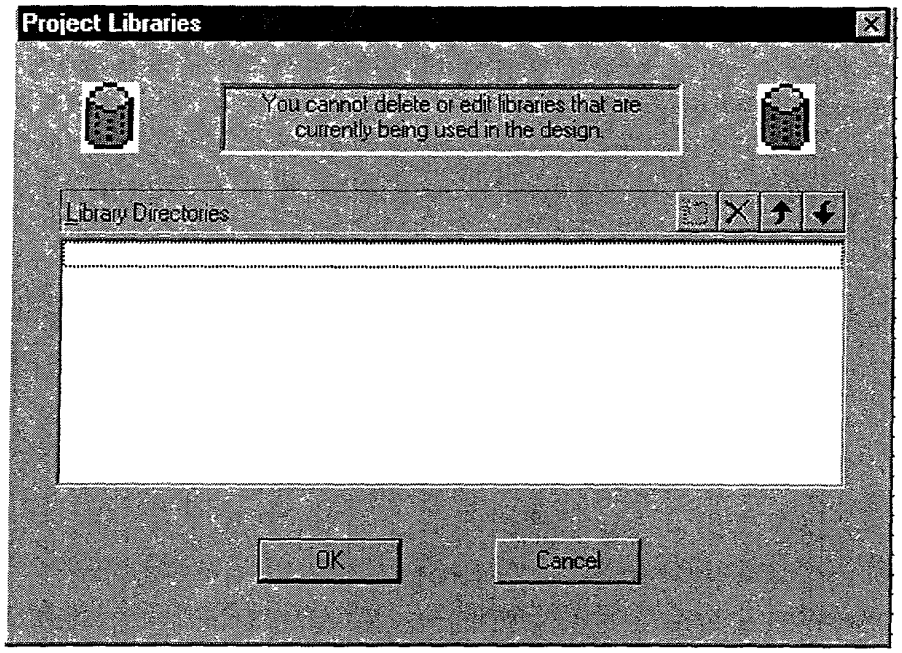


FIG.32

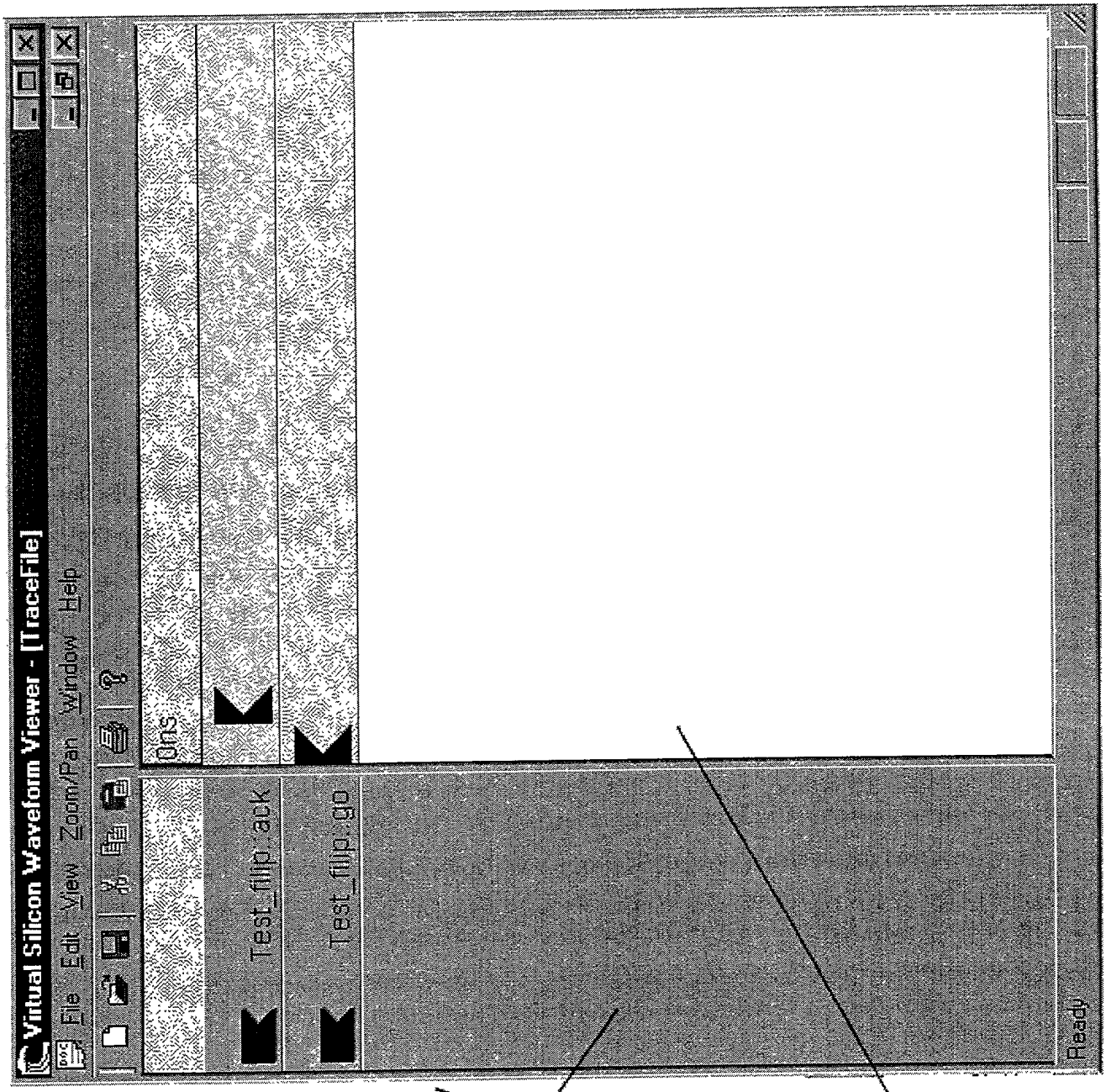

Virtual Silicon Waveform Viewer - [TraceFile]
File Edit View Zoom/Pan Window Help
Ons
Test_flip.ack
Test_flip.go
Ready
Name Display Window
Waveform Display

FIG. 33A

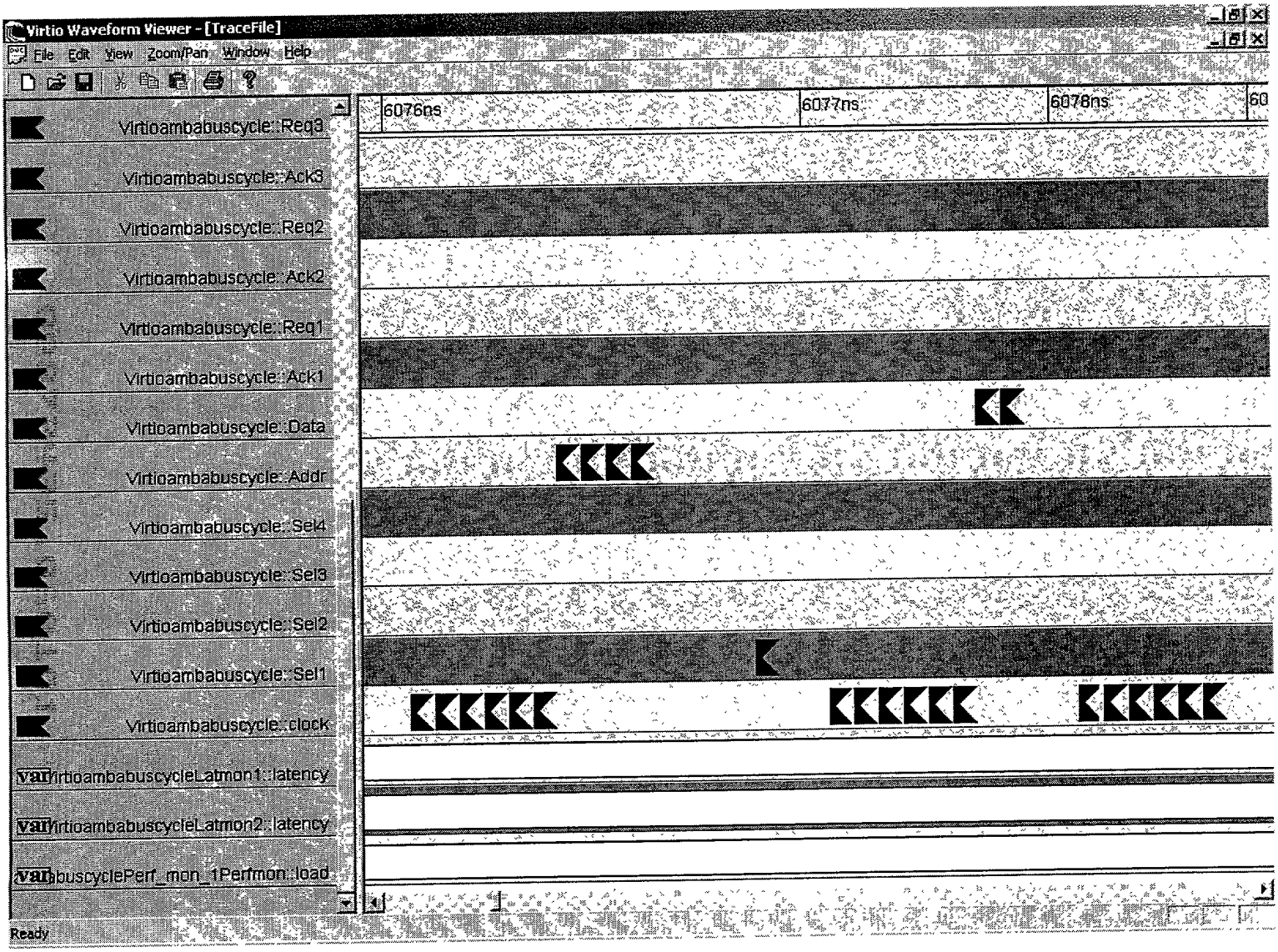

Virtio Waveform Viewer - [TraceFile]
File Edit View Zoom/Pan Window Help
Virtioambabuscycle::Req3
Virtioambabuscycle::Ack3
Virtioambabuscycle::Req2
Virtioambabuscycle::Ack2
Virtioambabuscycle::Req1
Virtioambabuscycle::Ack1
Virtioambabuscycle::Data
Virtioambabuscycle::Addr
Virtioambabuscycle::Sel4
Virtioambabuscycle::Sel3
Virtioambabuscycle::Sel2
Virtioambabuscycle::Sel1
Virtioambabuscycle::clock
var virtioambabuscycleLatmon1::latency
var virtioambabuscycleLatmon2::latency
var buscyclePerf_mon_1Perfmon::load
6076ns
6077ns
6078ns
Ready

FIG. 33B

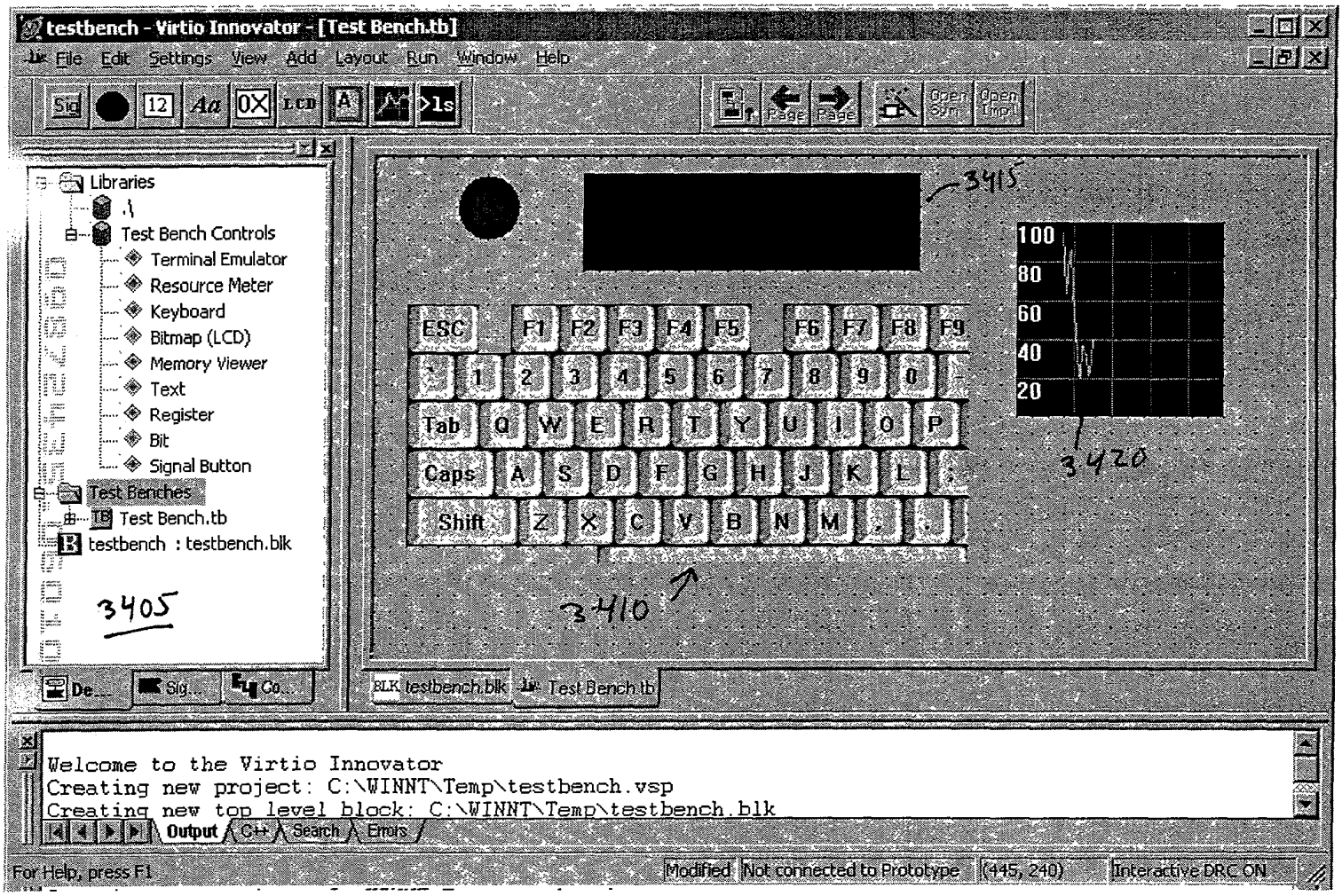

testbench - Virtio Innovator - [Test Bench.tb]
File Edit Settings View Add Layout Run Window Help
Libraries
.\
Test Bench Controls
Terminal Emulator
Resource Meter
Keyboard
Bitmap (LCD)
Memory Viewer
Text
Register
Bit
Signal Button
Test Benches
Test Bench.tb
testbench : testbench.blk
3405
3415
3420
3410
100
80
60
40
20
ESC F1 F2 F3 F4 F5 F6 F7 F8 F9
Tab Q W E R T Y U I O P
Caps A S D F G H J K L
Shift Z X C V B N M
BLK testbench.blk
Test Bench.tb
Welcome to the Virtio Innovator
Creating new project: C:\WINNT\Temp\testbench.vsp
Creating new top level block: C:\WINNT\Temp\testbench.blk
Output C++ Search Errors
For Help, press F1
Modified
Not connected to Prototype
(445, 240)
Interactive DRC ON

FIG. 34A

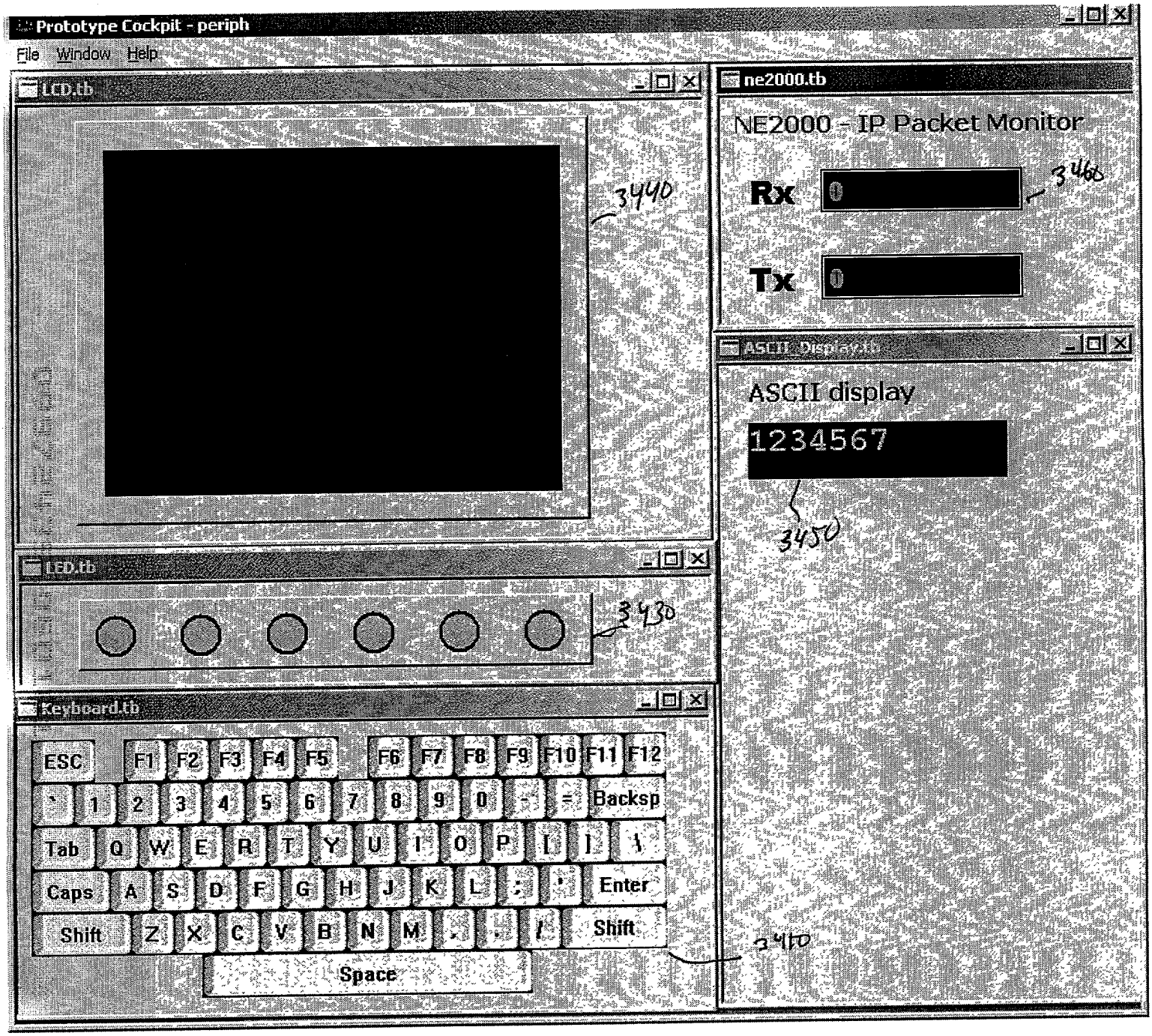

Prototype Cockpit - periph
File Window Help
LCD.tb
3440
LED.tb
3430
Keyboard.tb
ESC F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12
` 1 2 3 4 5 6 7 8 9 0 - = Backsp
Tab Q W E R T Y U I O P [ ] \
Caps A S D F G H J K L ; ' Enter
Shift Z X C V B N M , . / Shift
Space
3410
ne2000.tb
NE2000 - IP Packet Monitor
Rx 0
3460
Tx 0
ASCII Display
ASCII display
1234567
3450

FIG 34B

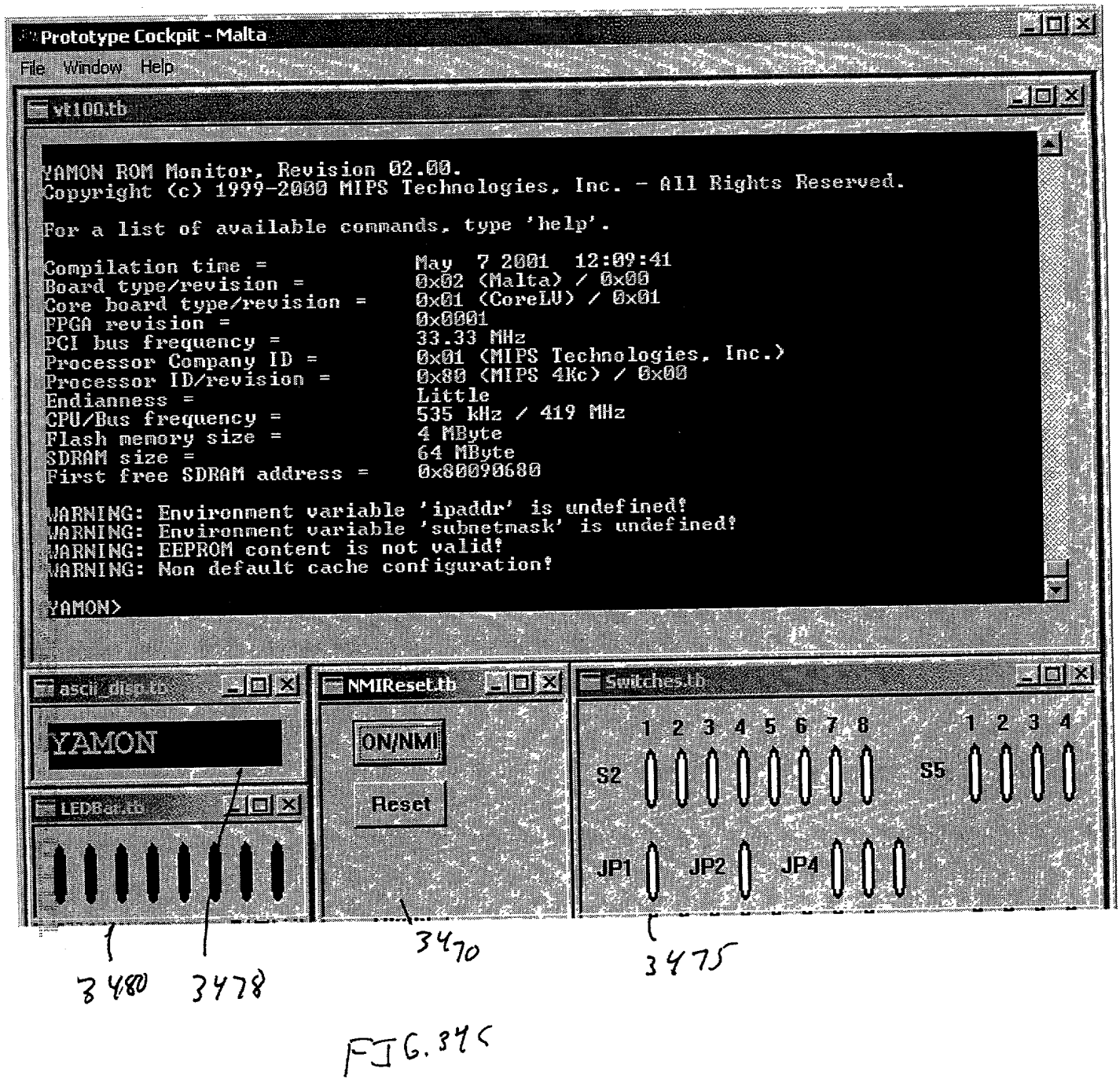

Prototype Cockpit - Malta
File Window Help
vt100.tb
YAMON ROM Monitor, Revision 02.00.
Copyright (c) 1999-2000 MIPS Technologies, Inc. - All Rights Reserved.
For a list of available commands, type 'help'.
Compilation time = May 7 2001 12:09:41
Board type/revision = 0x02 (Malta) / 0x00
Core board type/revision = 0x01 (CoreLV) / 0x01
FPGA revision = 0x0001
PCI bus frequency = 33.33 MHz
Processor Company ID = 0x01 (MIPS Technologies, Inc.)
Processor ID/revision = 0x80 (MIPS 4Kc) / 0x00
Endianness = Little
CPU/Bus frequency = 535 kHz / 419 MHz
Flash memory size = 4 MByte
SDRAM size = 64 MByte
First free SDRAM address = 0x80090680
WARNING: Environment variable 'ipaddr' is undefined!
WARNING: Environment variable 'subnetmask' is undefined!
WARNING: EEPROM content is not valid!
WARNING: Non default cache configuration!
YAMON>
YAMON
LEDBar.tb
NMIReset.tb
ON/NMI
Reset
Switches.tb
1 2 3 4 5 6 7 8
S2
1 2 3 4
S5
JP1
JP2
JP4
3480
3478
3470
3475

FIG. 34

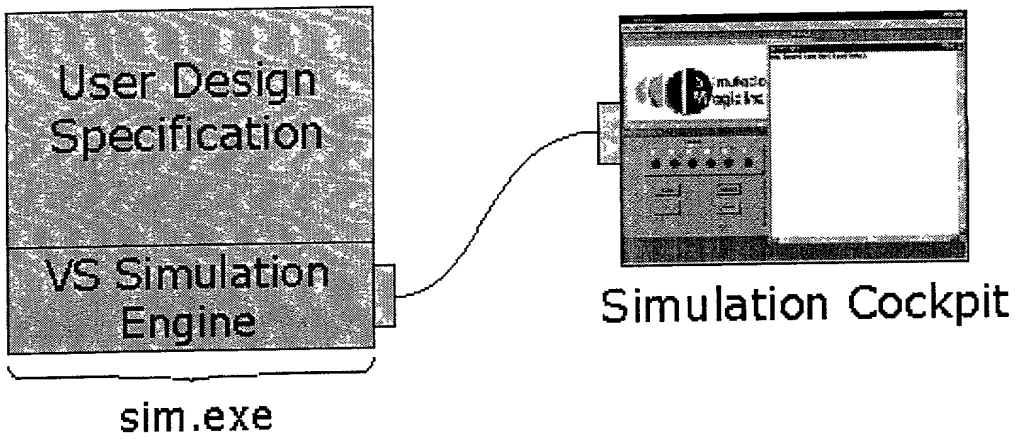

User Design Specification
VS Simulation Engine
sim.exe
Simulation Cockpit

FIG. 35

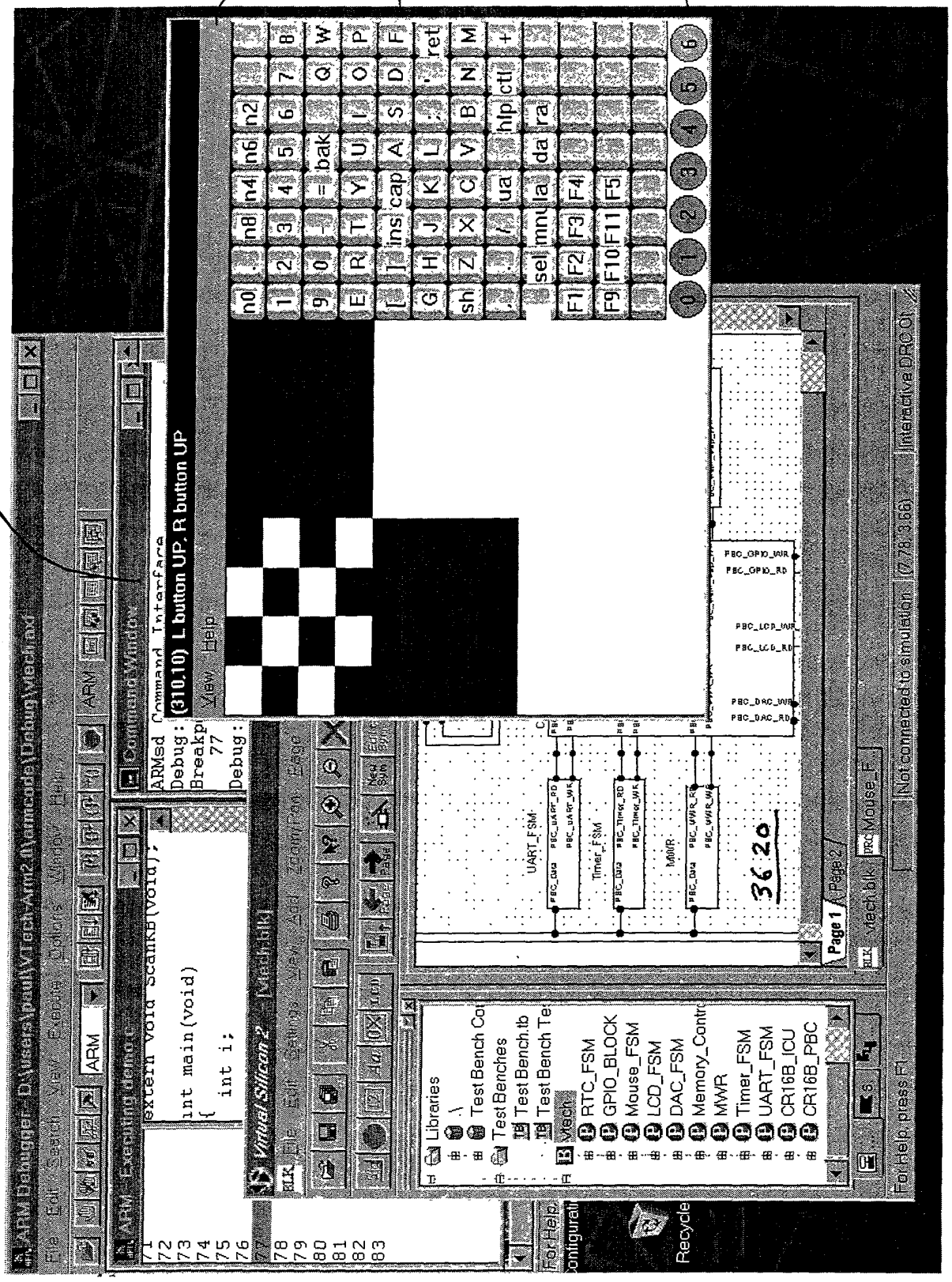


FIG. 36A

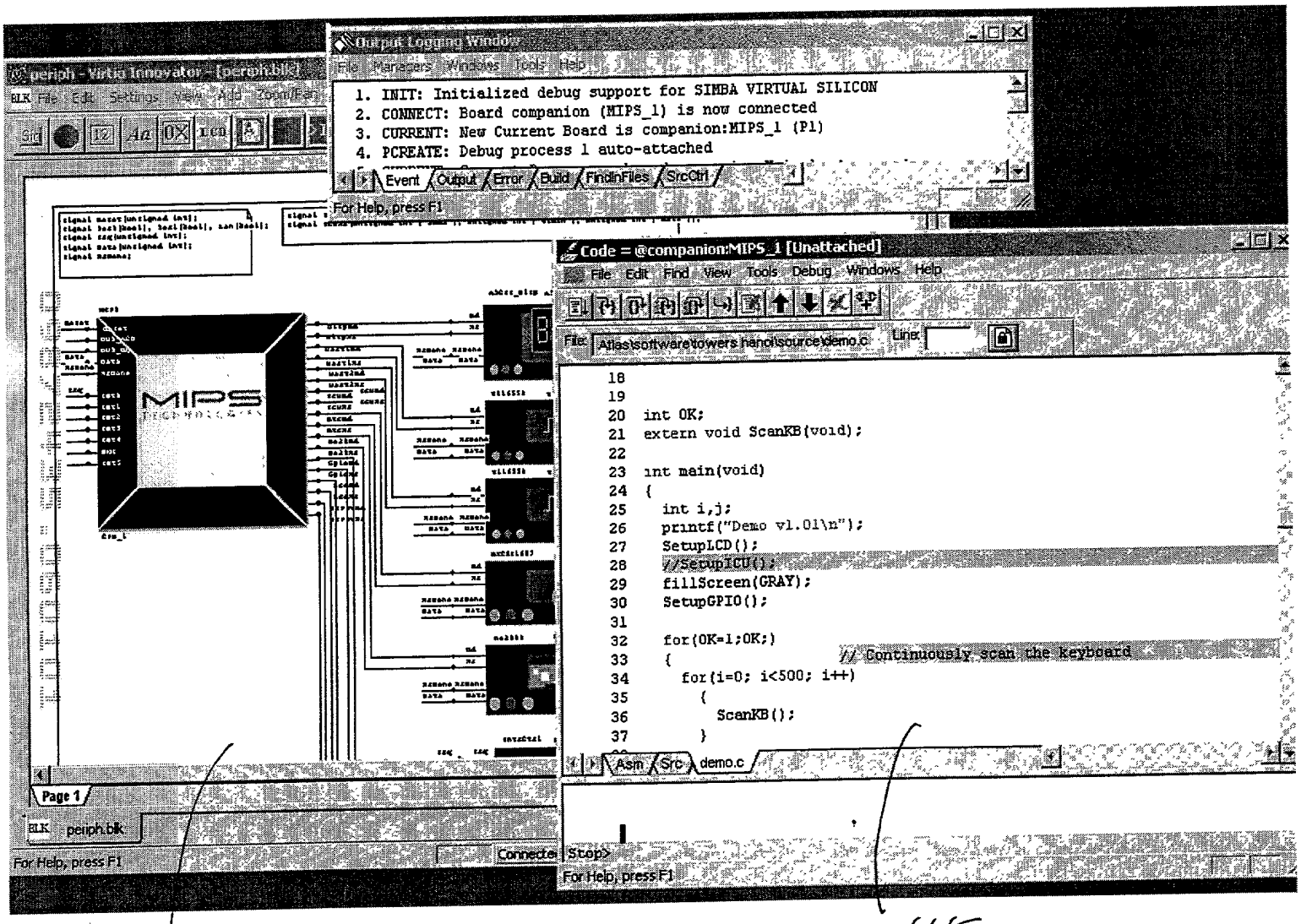

Output Logging Window
1. INIT: Initialized debug support for SIMBA VIRTUAL SILICON
2. CONNECT: Board companion (MIPS_1) is now connected
3. CURRENT: New Current Board is companion:MIPS_1 (P1)
4. PCREATE: Debug process 1 auto-attached
Event
Output
Error
Build
FindInFiles
SrcCtrl
For Help, press F1
Code = @companion:MIPS_1 [Unattached]
File Edit Find View Tools Debug Windows Help
File: Atlas\software\towers hand\source\demo.c
Line:
18
19
20 int OK;
21 extern void ScanKB(void);
22
23 int main(void)
24 {
25 int i,j;
26 printf("Demo v1.01\n");
27 SetupLCD();
28 //SetupICU();
29 fillScreen(GRAY);
30 SetupGPIO();
31
32 for(OK=1;OK;)
33 { // Continuously scan the keyboard
34 for(i=0; i<500; i++)
35 {
36 ScanKB();
37 }
Asm
Src
demo.c
Page 1
BLK periph.blk
For Help, press F1
Connected
Stop>
For Help, press F1
3620
3685

FIG. 36B

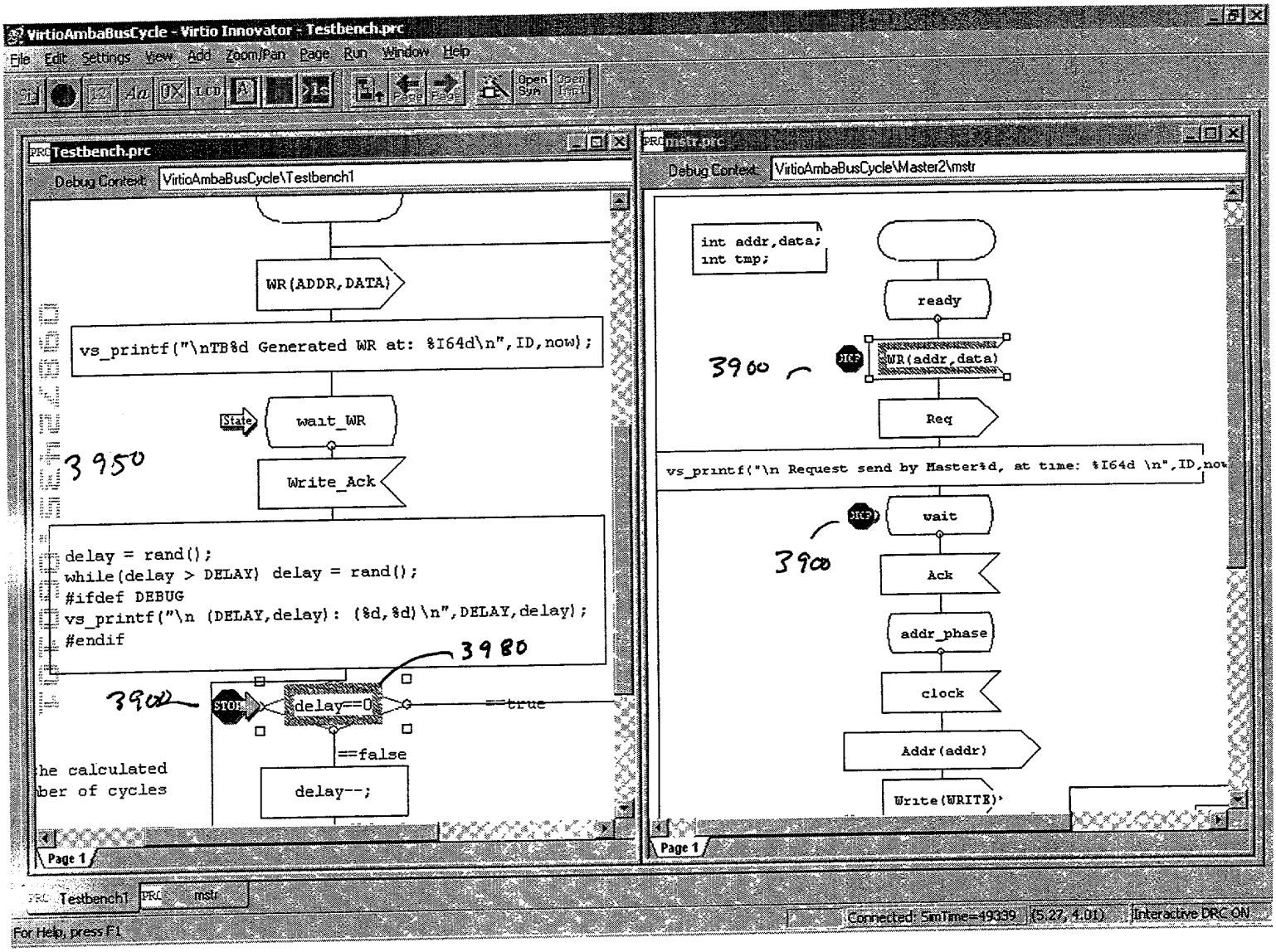

VirtioAmbaBusCycle - Virtio Innovator - Testbench.prc
File Edit Settings View Add Zoom/Pan Page Run Window Help
Testbench.prc
Debug Context: VirtioAmbaBusCycle\Testbench1
WR(ADDR,DATA)
vs_printf("\nTB%d Generated WR at: %I64d\n",ID,now);
State
wait_WR
Write_Ack
3950
delay = rand();
while(delay > DELAY) delay = rand();
#ifdef DEBUG
vs_printf("\n (DELAY,delay): (%d,%d)\n",DELAY,delay);
#endif
3980
3900
STOP
delay==0
==true
==false
delay--;
he calculated
ber of cycles
Page 1
Debug Context: VirtioAmbaBusCycle\Master2\mstr
int addr,data;
int tmp;
ready
3900
WR(addr,data)
Req
vs_printf("\n Request send by Master%d, at time: %I64d \n",ID,now
wait
3900
Ack
addr_phase
clock
Addr(addr)
Write(WRITE)
Page 1
Testbench1
mstr
For Help, press F1
Connected: SimTime=49339
(5.27, 4.01)
Interactive DRC ON

FIG. 36C

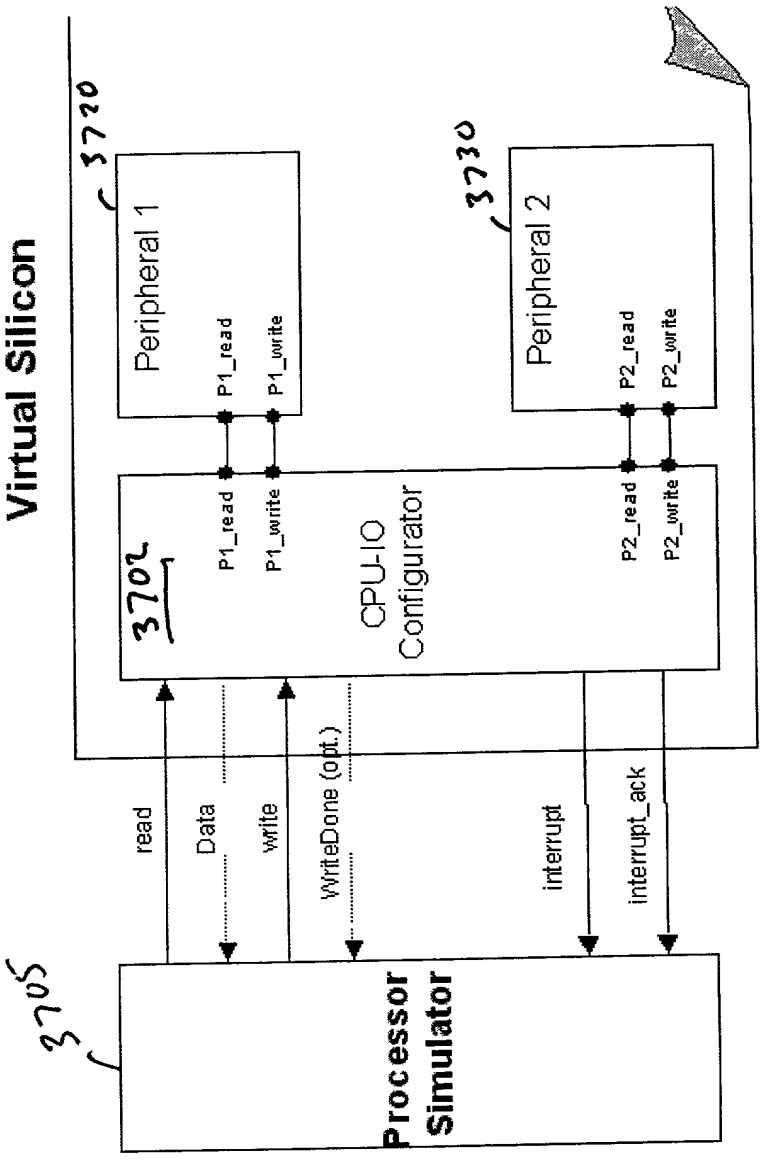

Virtual Silicon
3720
Peripheral 1
P1_read
P1_write
3730
Peripheral 2
P2_read
P2_write
3702
CPU-IO Configurator
P1_read
P1_write
P2_read
P2_write
read
Data
write
WriteDone (opt.)
interrupt
interrupt_ack
3705
Processor Simulator

FIG. 37

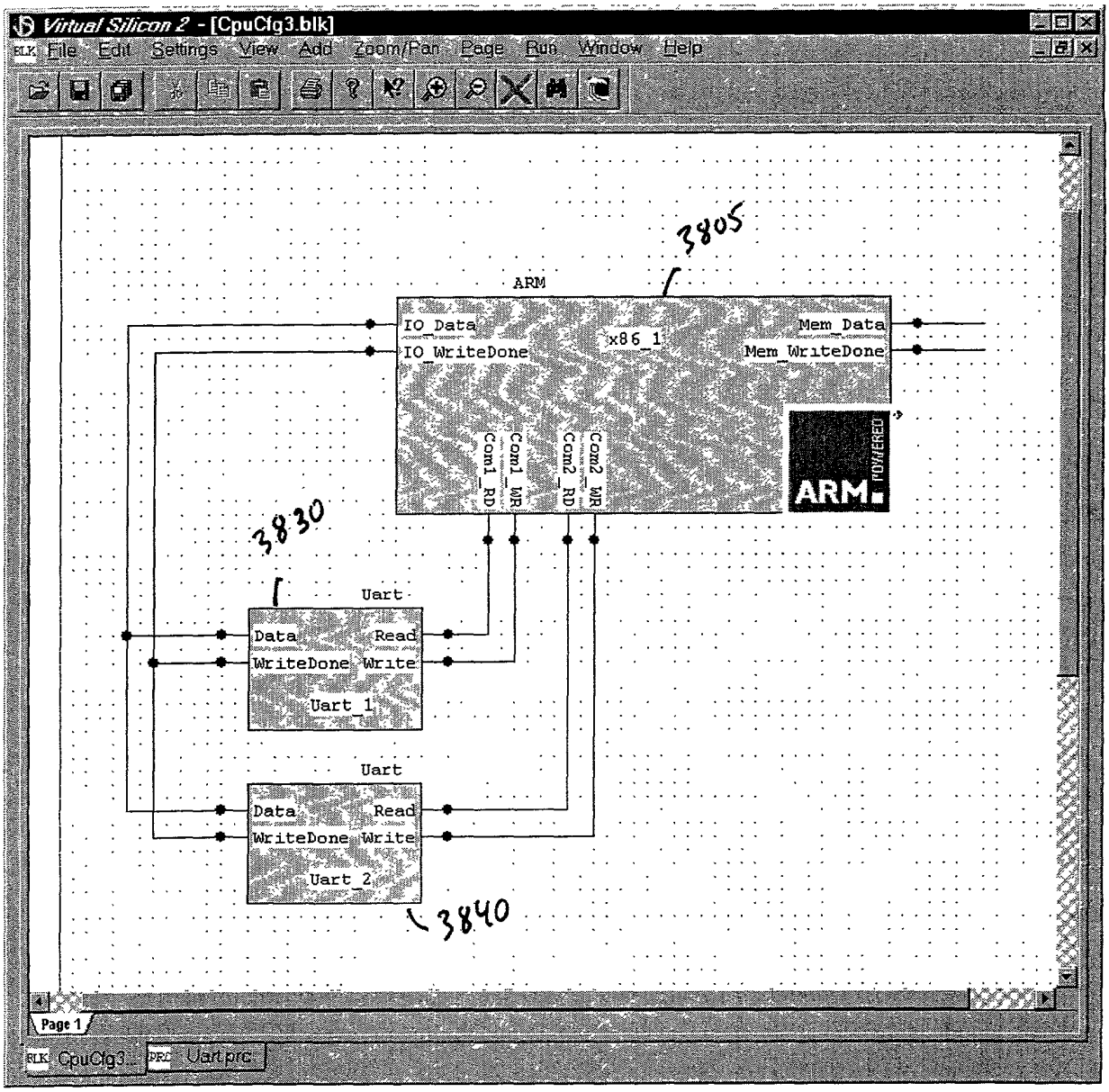

Virtual Silicon 2 - [CpuCfg3.blk]
File Edit Settings View Add Zoom/Pan Page Run Window Help
3805
ARM
IO_Data
IO_WriteDone
x86_1
Mem_Data
Mem_WriteDone
Com1_RD
Com1_WR
Com2_RD
Com2_WR
ARM
3830
Uart
Data
WriteDone
Read
Write
Uart_1
Uart
Data
WriteDone
Read
Write
Uart_2
3840
Page 1
CpuCfg3
Uartprc

FIG. 38

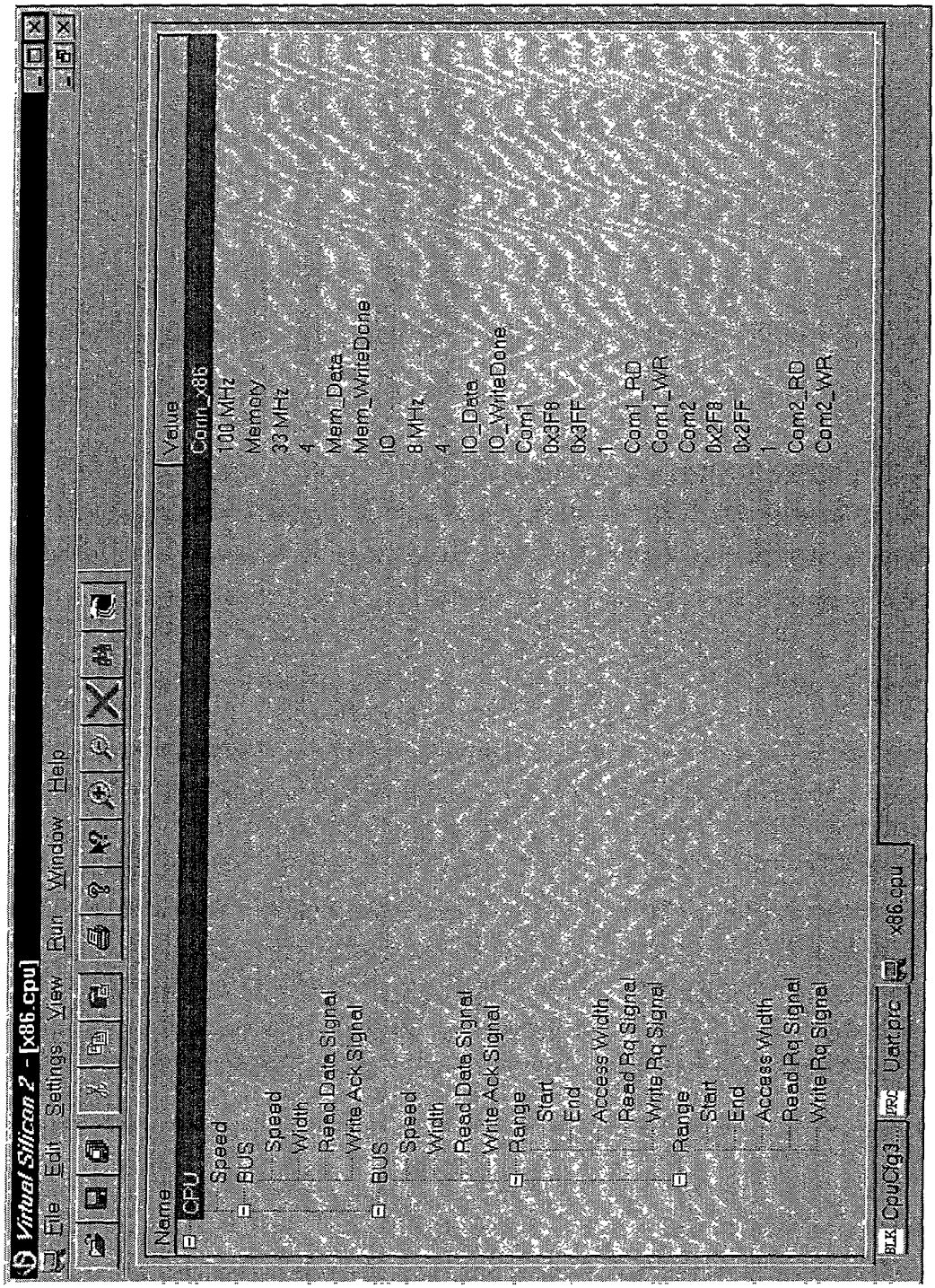

Virtual Silicon 2 - [x86.cpu]
File Edit Settings View Run Window Help
Name
Value
CPU
Conn_x86
Speed
100 MHz
BUS
Memory
Speed
33 MHz
Width
4
Read Data Signal
Mem_Data
Write Ack Signal
Mem_WriteDone
BUS
IO
Speed
8 MHz
Width
4
Read Data Signal
IO_Data
Write Ack Signal
IO_WriteDone
Range
Com1
Start
0x3F8
End
0x3FF
Access Width
1
Read Rq Signal
Com1_RD
Write Rq Signal
Com1_WR
Range
Com2
Start
0x2F8
End
0x2FF
Access Width
1
Read Rq Signal
Com2_RD
Write Rq Signal
Com2_WR
CpuCfg1.inc
Uart.prc
x86.cpu

FIG. 39

Name	Value
⊟ CPU	ArmCPU
Speed	100 MHz
⊟ Events: CPU -> Simulation	
RESET Signal	Reset
BUS_ACK Signal	Bus_ACK
⊟ Events: Simulation -> CPU	
BUS_RQ	Bus_RQ
⊟ Interrupt Support	Yes
FIRQ Signal	FIQ
IRQ Signal	IRQ
⊟ BUS	Memory
Speed	100 MHz
Width	4
Read Data Signal	Read_Data
⊟ Write Timing	Variable
Write Ack Signal	Write_Ack
⊟ Range	Counter
Type	Slave
Start	CNT_START_ADDR
End	CNT_END_ADDR
Access Width	4
Read Rq Signal	CNT_RD
Write Rq Signal	CNT_WR

FIG. 40

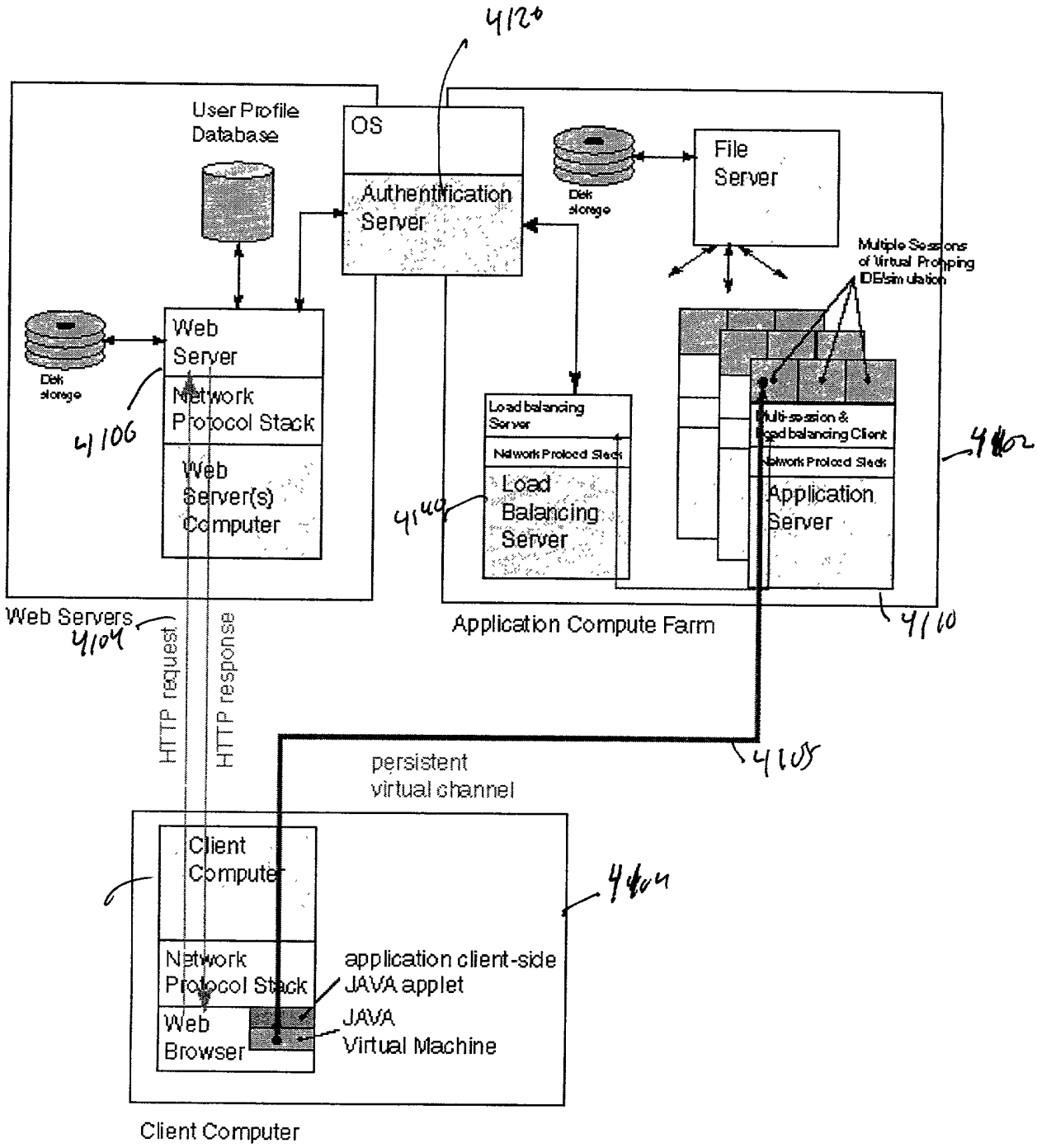

4120
User Profile Database
OS
Authentification Server
Disk storage
File Server
Multiple Sessions of Virtual Prototyping DB Simulation
Web Server
Network Protocol Stack
Web Server(s) Computer
Disk storage
4106
Load balancing Server
Network Protocol Stack
Load Balancing Server
4140
Multi-session & Load balancing Client
Network Protocol Stack
Application Server
4102
Web Servers
4104
Application Compute Farm
4110
HTTP request
HTTP response
persistent virtual channel
4105
Client Computer
Network Protocol Stack
Web Browser
application client-side JAVA applet
JAVA Virtual Machine
4104
Client Computer

FIG. 41

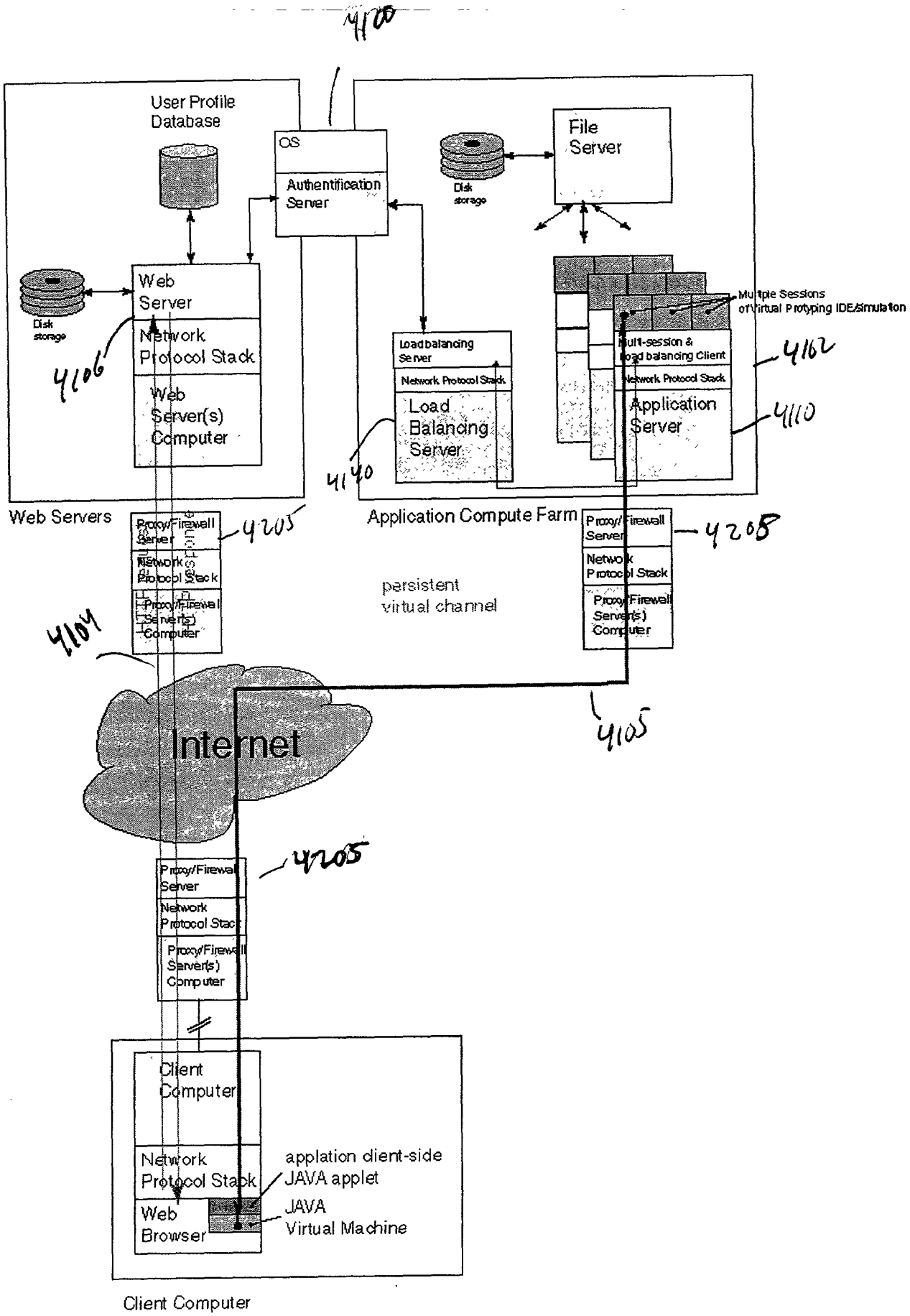

4100
User Profile Database
OS
Authentification Server
File Server
Disk storage
Disk storage
Web Server
Network Protocol Stack
Web Server(s) Computer
4106
Load balancing Server
Network Protocol Stack
Load Balancing Server
4140
Multiple Sessions of Virtual Protyping IDE/Simulation
Multi-session & load balancing Client
Network Protocol Stack
Application Server
4162
4110
Web Servers
Application Compute Farm
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4205
4208
persistent virtual channel
4104
Internet
4105
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4205
Client Computer
Network Protocol Stack
Web Browser
applation client-side JAVA applet
JAVA Virtual Machine
Client Computer

FIG. 42

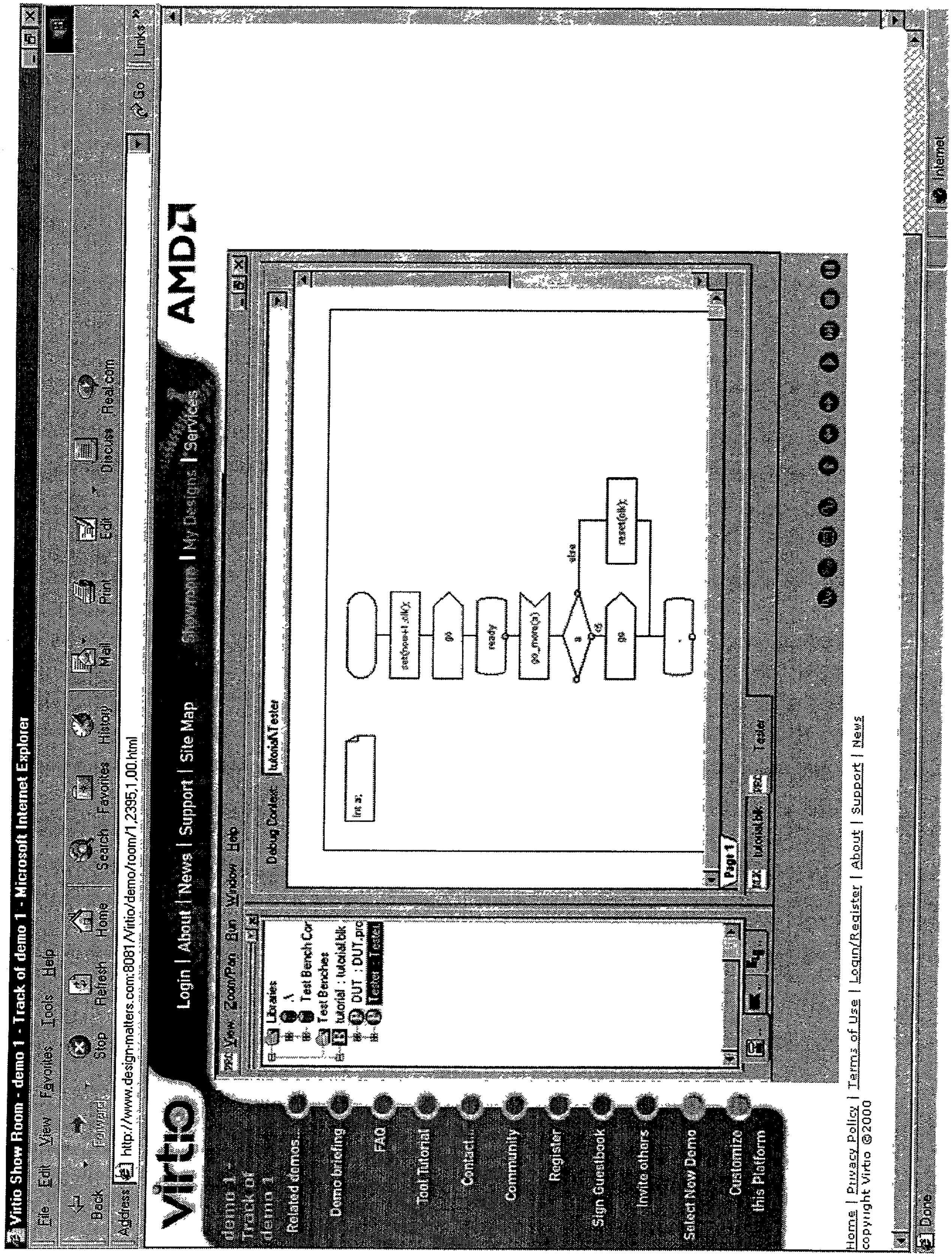

Virtio Show Room - demo 1 - Track of demo 1 - Microsoft Internet Explorer
File Edit View Favorites Tools Help
Back Forward Stop Refresh Home Search Favorites History Mail Print Edit Discuss Real.com
Address http://www.design-matters.com:8081/virtio/demo/room/1,2395,1,00.html
Go Links
virtio
Login | About | News | Support | Site Map
Showrooms | My Designs | Services
AMD
demo 1 - Track of demo 1
Related demos...
Demo briefing
FAQ
Tool Tutorial
Contact...
Community
Register
Sign Guestbook
Invite others
Select New Demo
Customize this Platform
View Zoom/Pan Run Window Help
Libraries
Test Bench Cor
Test Benches
tutorial : tutorial.blk
DUT : DUT.pro
Tester : Tester
Debug Context: tutorialATester
int a;
go
ready
go_more(a)
else
reset(clk);
go
Page 1
tutorial.blk
Tester
Home | Privacy Policy | Terms of Use | Login/Register | About | Support | News
copyright Virtio ©2000
Done
Internet

FIG-43

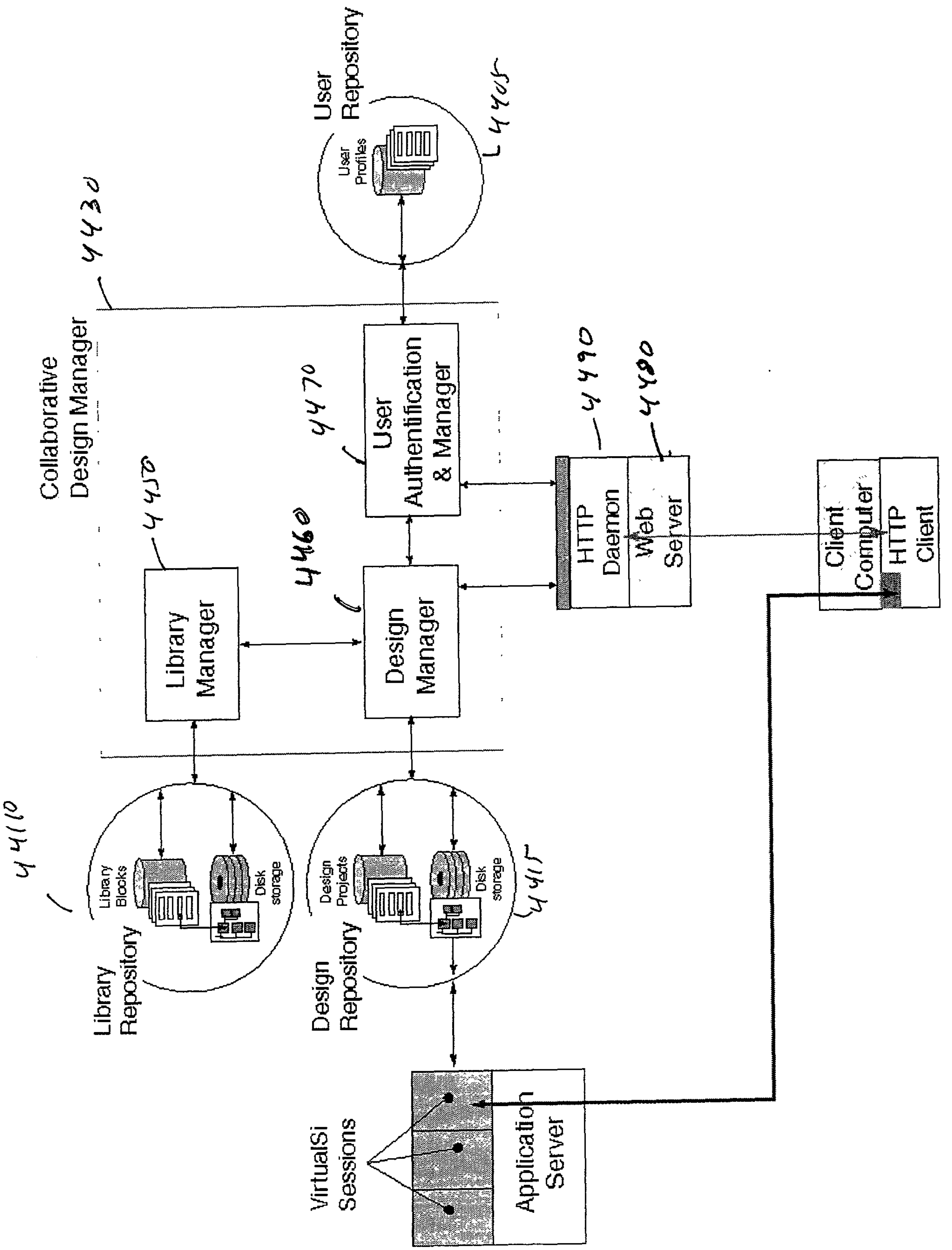

Collaborative Design Manager
4430
User Repository
User Profiles
4405
User Authentification & Manager
4470
Library Manager
4450
Design Manager
4460
HTTP Daemon
4490
Web Server
4480
Client Computer
HTTP Client
Library Repository
Library Blocks
Disk storage
4410
Design Repository
Design Projects
Disk storage
4415
VirtualSi Sessions
Application Server

FIG. 44

{} Clock_1	Scope name.
clk(int)	Signal name and declaration.

t	Timer or clock name and declaration.
clk	Local name of a signal coming from the upper scope (inherited).
myClk	Timer or clock is being set.
	Signal is being sent.
	Signal is being received.
	Signal is being saved.

FIG. 45

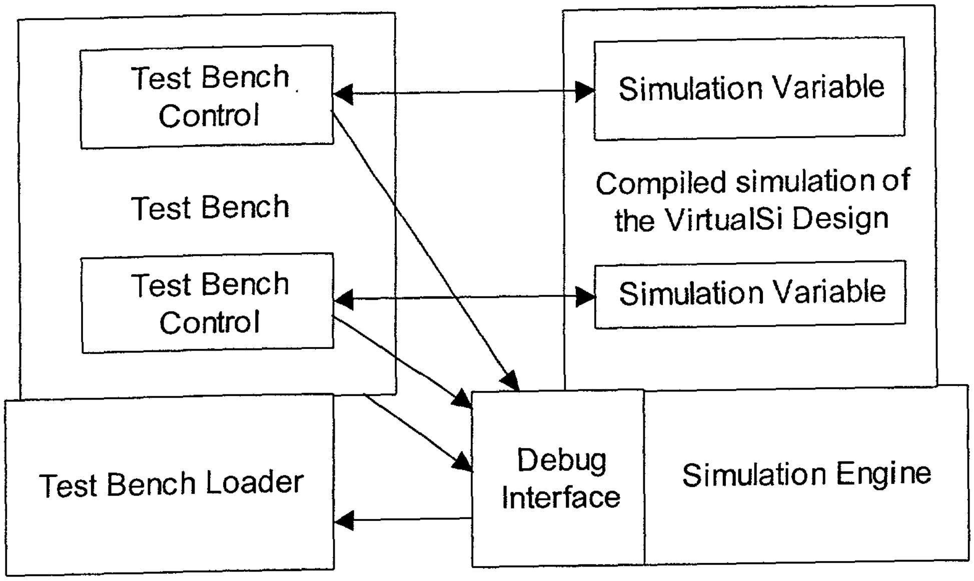

Test Bench Control
Test Bench
Test Bench Control
Simulation Variable
Compiled simulation of the VirtualSi Design
Simulation Variable
Test Bench Loader
Debug Interface
Simulation Engine

FIG. 46

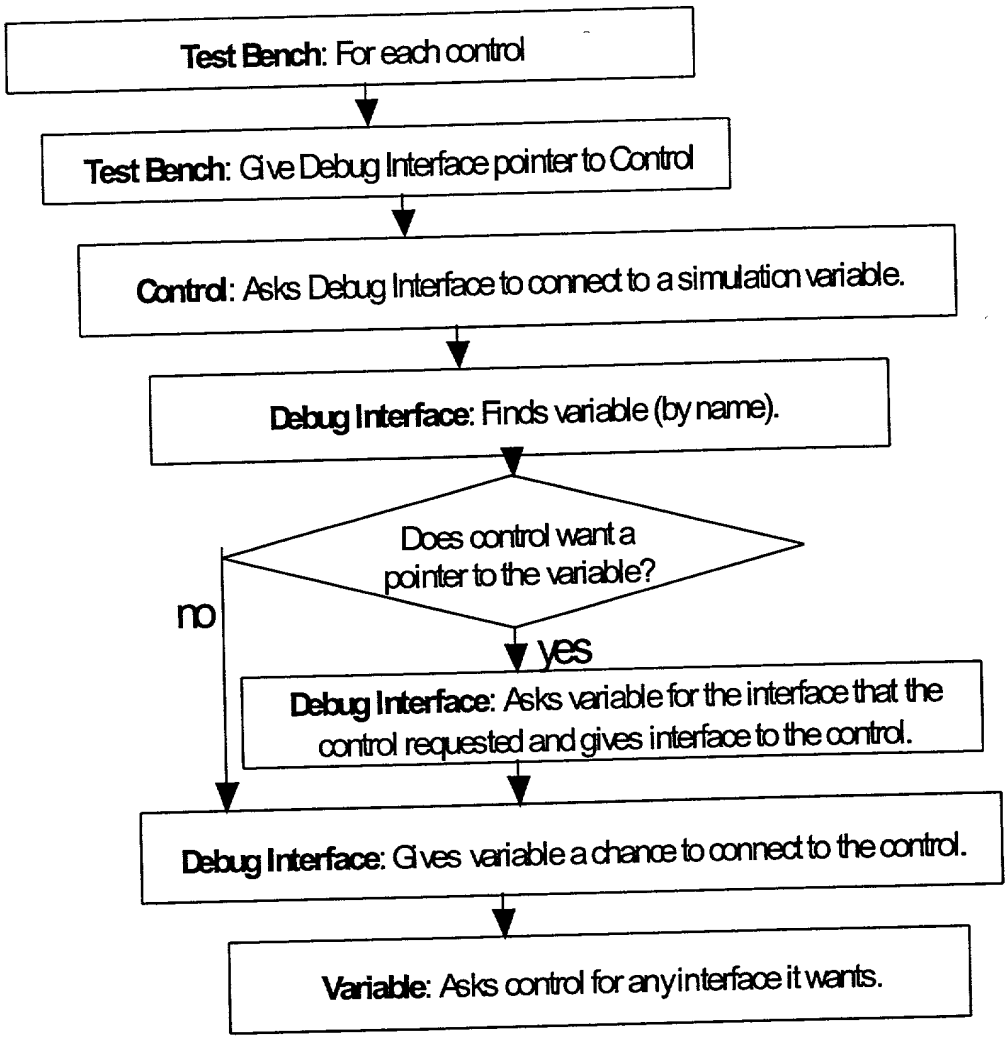

Test Bench: For each control
Test Bench: Give Debug Interface pointer to Control
Control: Asks Debug Interface to connect to a simulation variable.
Debug Interface: Finds variable (by name).
Does control want a pointer to the variable?
no
yes
Debug Interface: Asks variable for the interface that the control requested and gives interface to the control.
Debug Interface: Gives variable a chance to connect to the control.
Variable: Asks control for any interface it wants.

FIG. 47

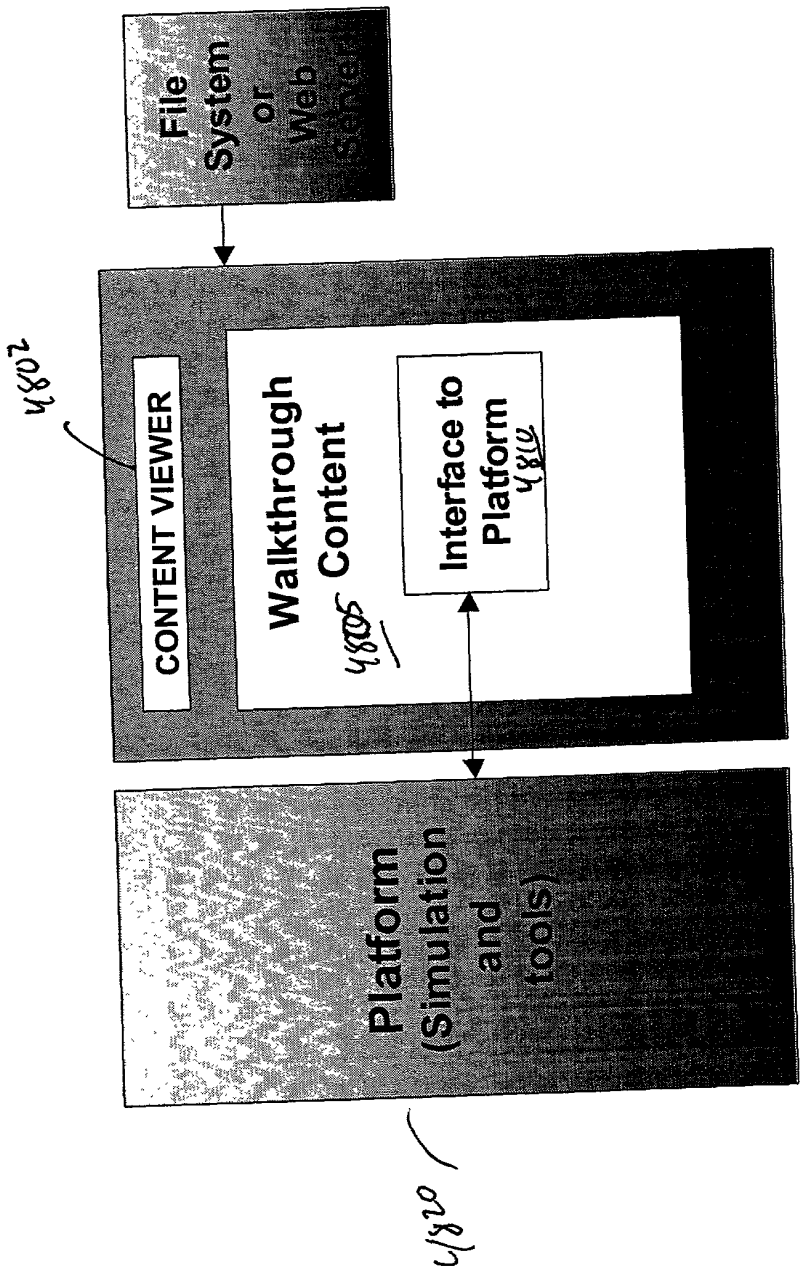

File System or Web Server
CONTENT VIEWER
Walkthrough Content
Interface to Platform
Platform (Simulation and tools)
4802
4804
4806
4808
4810

Fig. 48

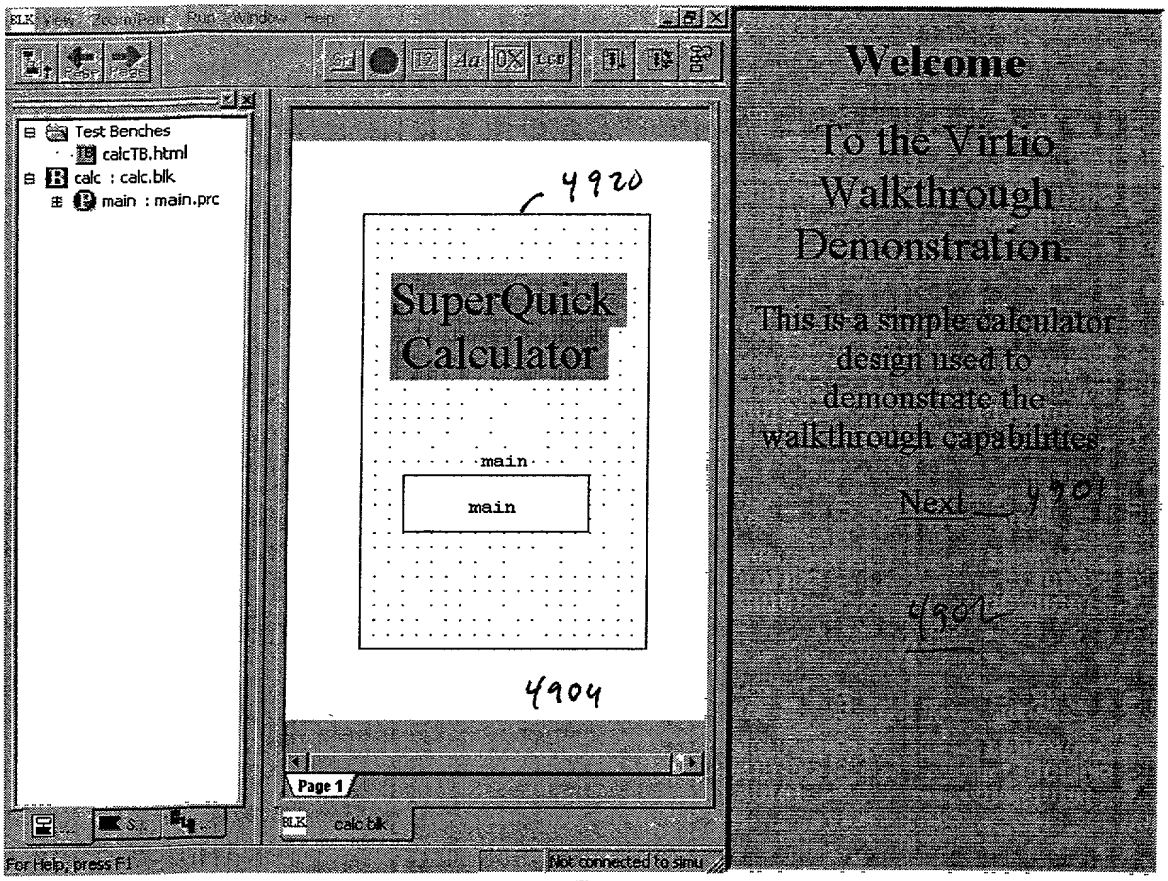

Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4920
SuperQuick Calculator
main
main
4904
Page 1
calc.blk
For Help, press F1
Not connected to simu
Welcome
To the Virtio Walkthrough Demonstration
This is a simple calculator design used to demonstrate the walkthrough capabilities.
Next
4902
4906

FIG. 49A

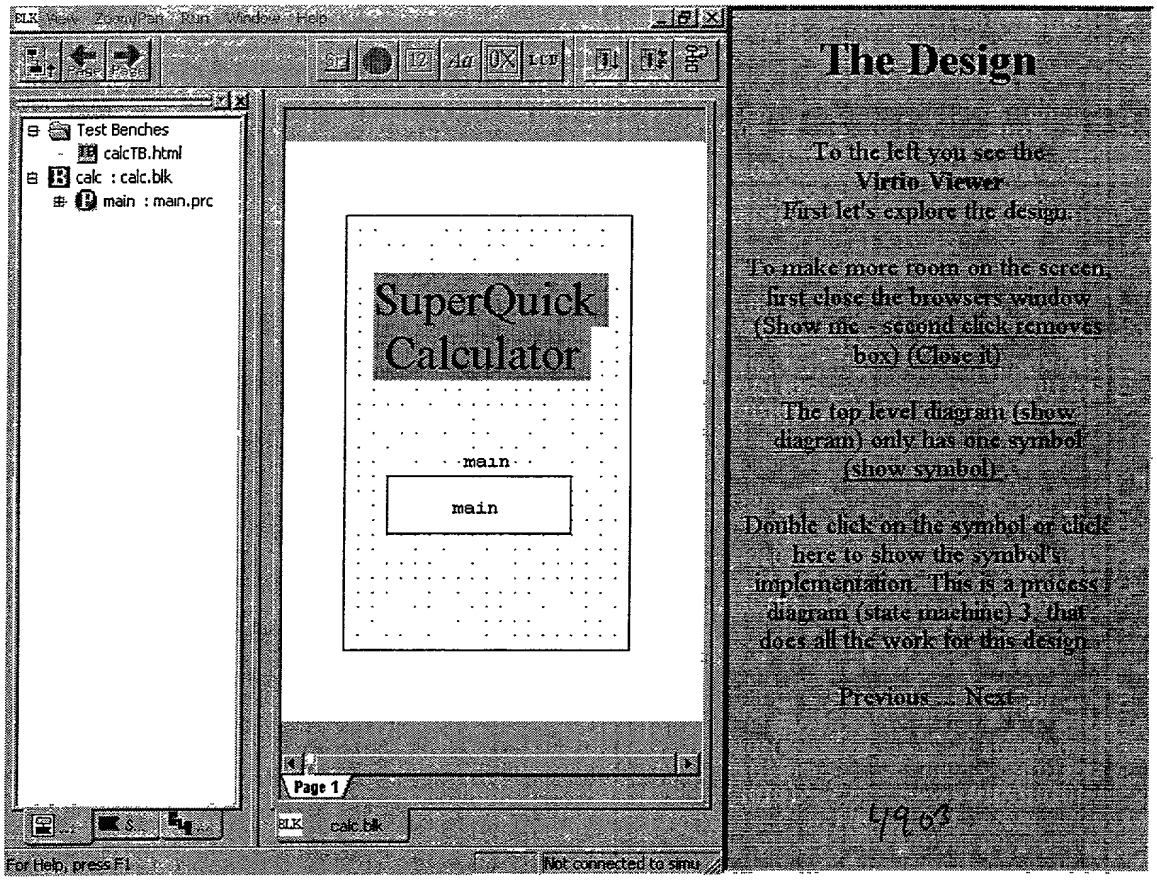


FIG. 49B

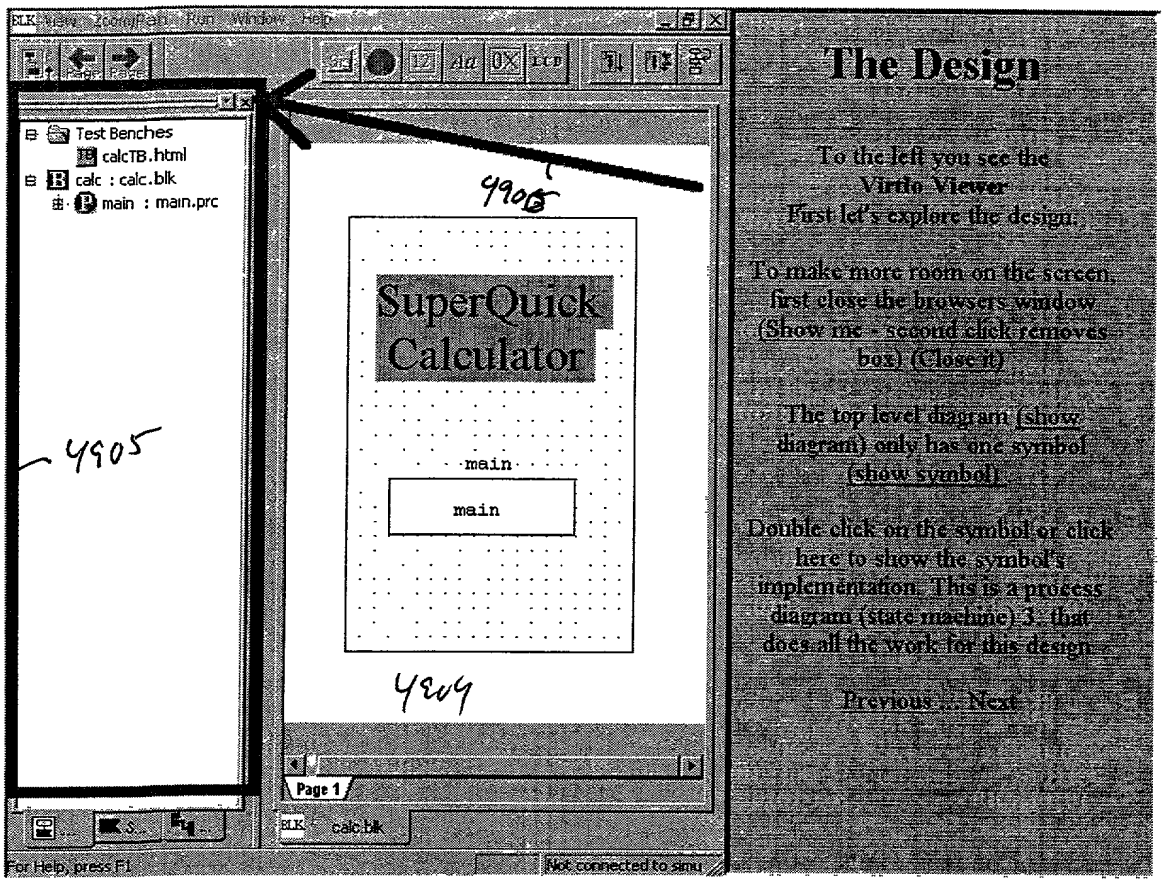


FIG. 49C

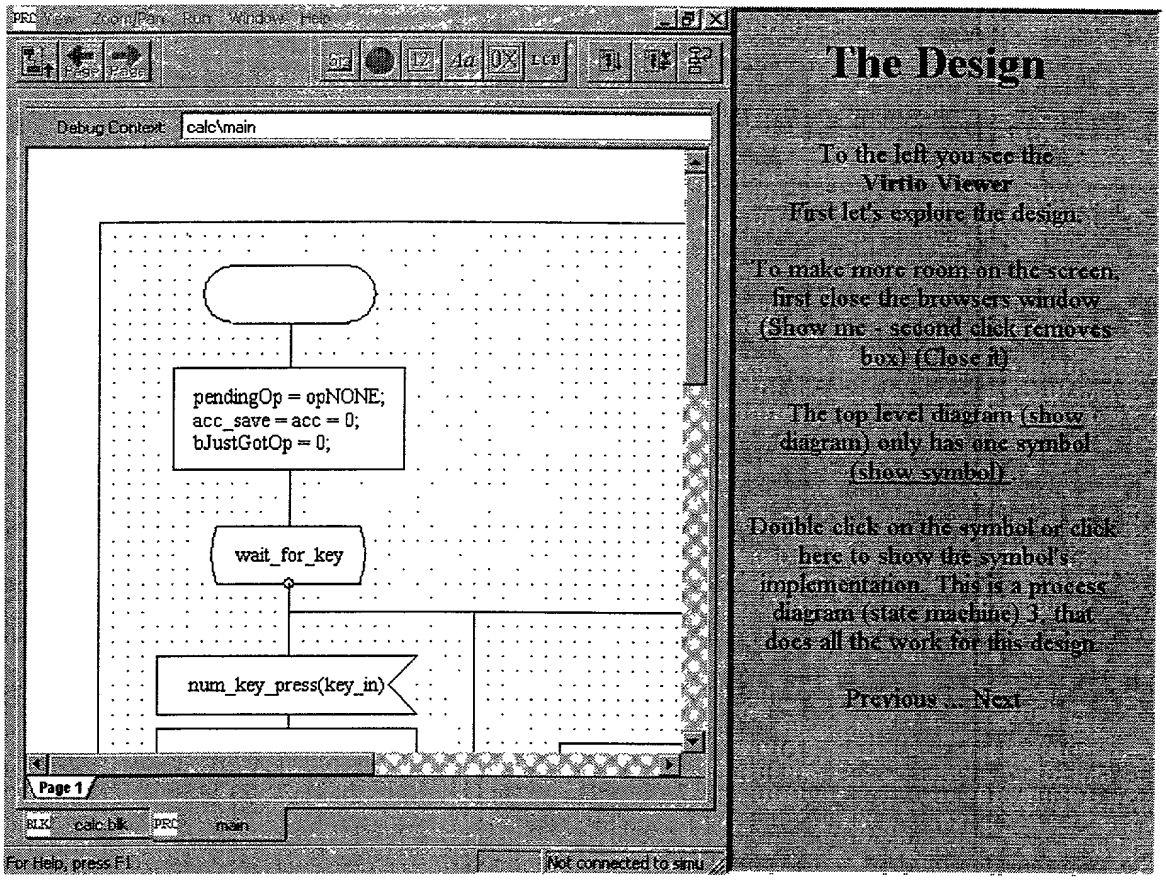

Debug Context: calc\main
pendingOp = opNONE;
acc_save = acc = 0;
bJustGotOp = 0;
wait_for_key
num_key_press(key_in)
Page 1
BLK calc.blk
PRC main
For Help, press F1
Not connected to simu
The Design
To the left you see the Virtio Viewer
First let's explore the design.
To make more room on the screen, first close the browsers window (Show me - second click removes box) (Close it)
The top level diagram (show diagram) only has one symbol (show symbol).
Double click on the symbol or click here to show the symbol's implementation. This is a process diagram (state machine) 3. that does all the work for this design.
Previous ... Next

FIG. 49 D

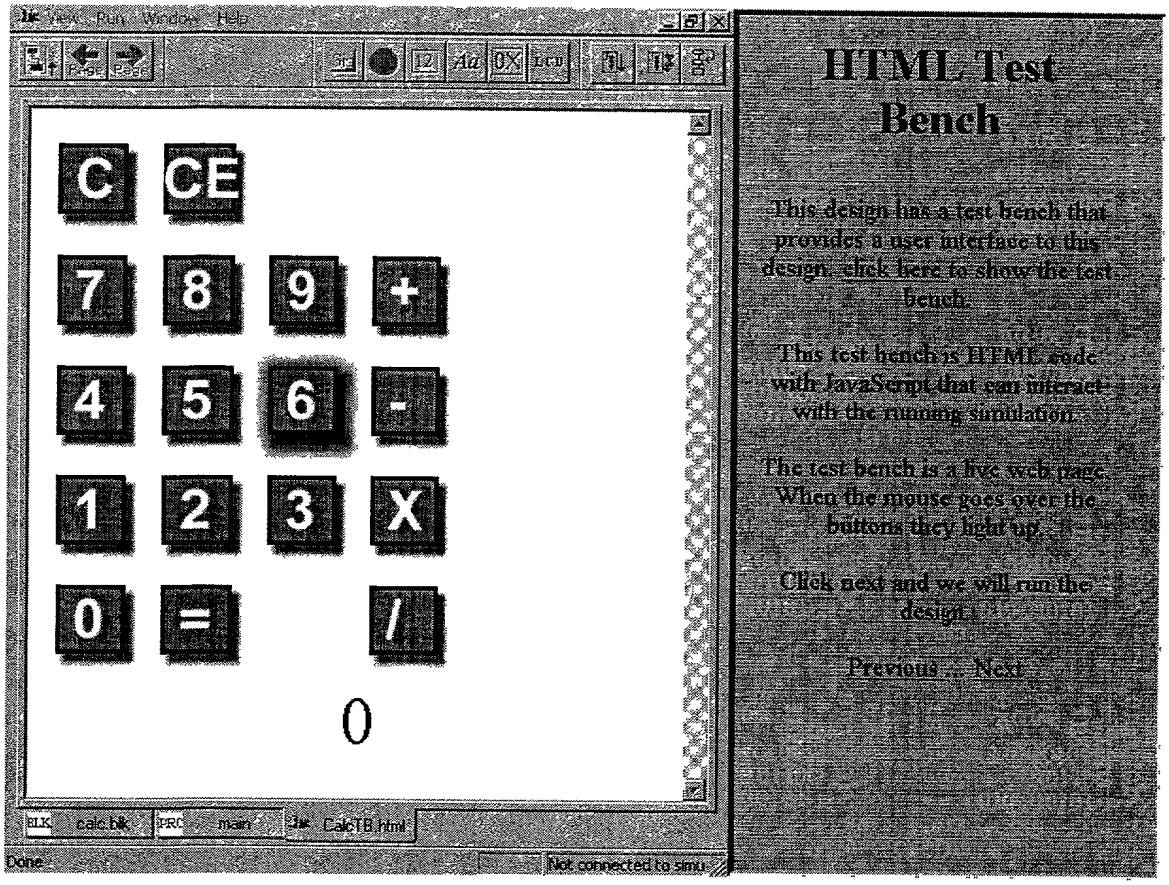

C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
0
calc.bk
main
CalcTB.html
Done
Not connected to simu
HTML Test Bench
This design has a test bench that provides a user interface to this design. click here to show the test bench.
This test bench is HTML code with JavaScript that can interact with the running simulation.
The test bench is a free web page. When the mouse goes over the buttons they light up.
Click next and we will run the design.
Previous ... Next

FIG. 49E

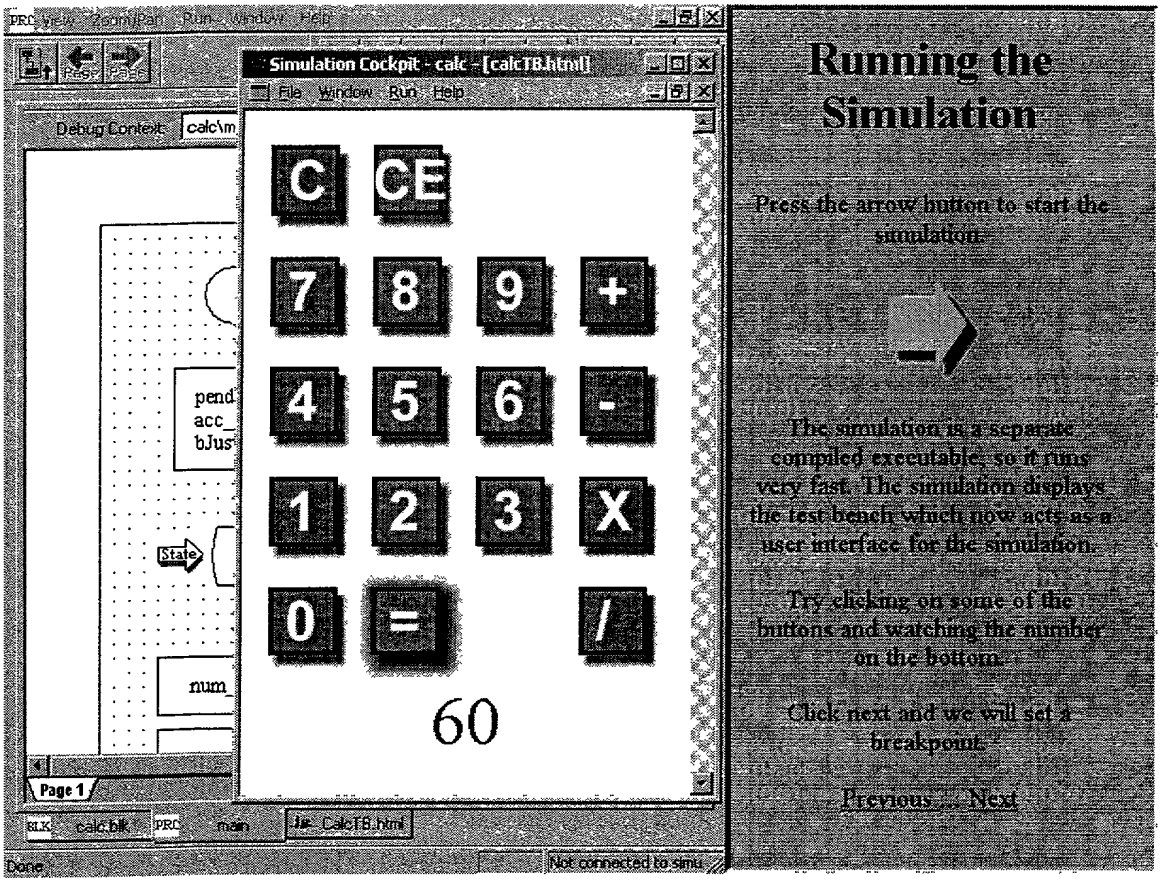

Simulation Cockpit - calc - [calcTB.html]
File Window Run Help
Debug Context
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
60
Page 1
Done
Not connected to simu
Running the Simulation
Press the arrow button to start the simulation.
The simulation is a separate compiled executable, so it runs very fast. The simulation displays the test bench which now acts as a user interface for the simulation.
Try clicking on some of the buttons and watching the number on the bottom.
Click next and we will set a breakpoint.
Previous Next

FIG. 49F

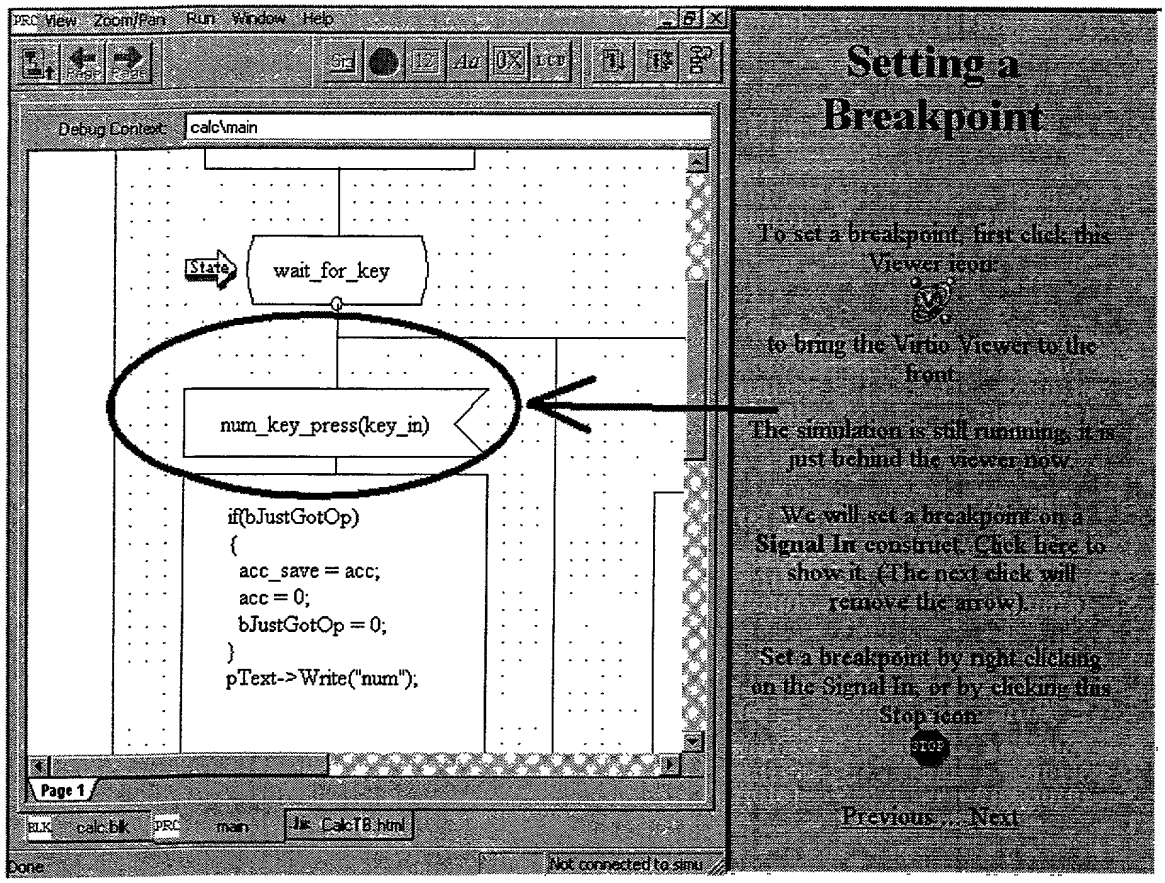

PRC View Zoom/Pan Run Window Help
Debug Context: calc\main
State
wait_for_key
num_key_press(key_in)
if(bJustGotOp)
{
acc_save = acc;
acc = 0;
bJustGotOp = 0;
}
pText->Write("num");
Page 1
BLK calc.blk
PRC main
calcTB.html
Done
Not connected to simu
Setting a Breakpoint
To set a breakpoint, first click this Viewer icon:
to bring the Virtio Viewer to the front.
The simulation is still running, it's just behind the viewer now.
We will set a breakpoint on a Signal In construct. Click here to show it. (The next click will remove the arrow).
Set a breakpoint by right clicking on the Signal In, or by clicking this Stop icon:
STOP
Previous... Next

FIG. 49G

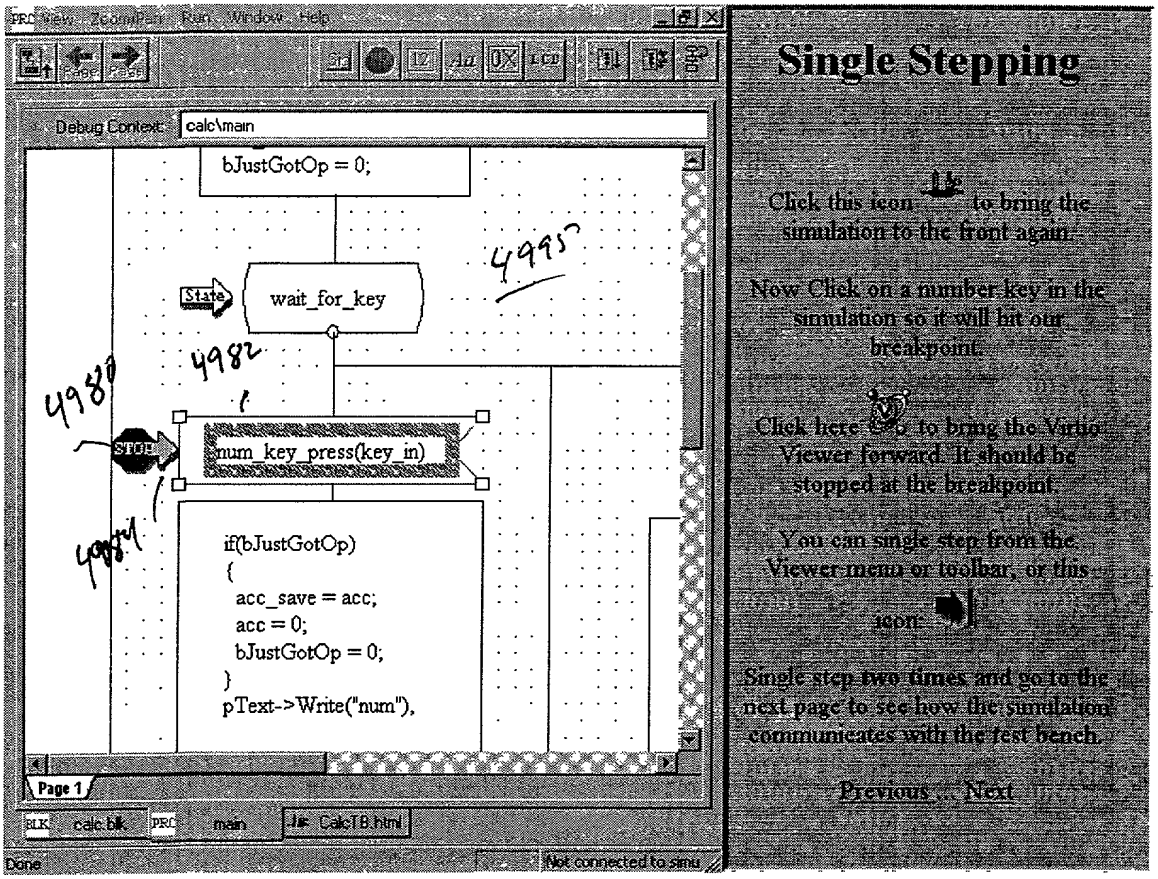

Debug Context: calc\main
bJustGotOp = 0;
State
wait_for_key
4995
4982
4983
STOP
num_key_press(key_in)
4984
if(bJustGotOp)
{
acc_save = acc;
acc = 0;
bJustGotOp = 0;
}
pText->Write("num"),
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simu
Single Stepping
Click this icon to bring the simulation to the front again.
Now Click on a number key in the simulation so it will hit our breakpoint.
Click here to bring the Virtio Viewer forward. It should be stopped at the breakpoint.
You can single step from the Viewer menu or toolbar, or this icon:
Single step two times and go to the next page to see how the simulation communicates with the test bench.
Previous
Next

FIG. 49H

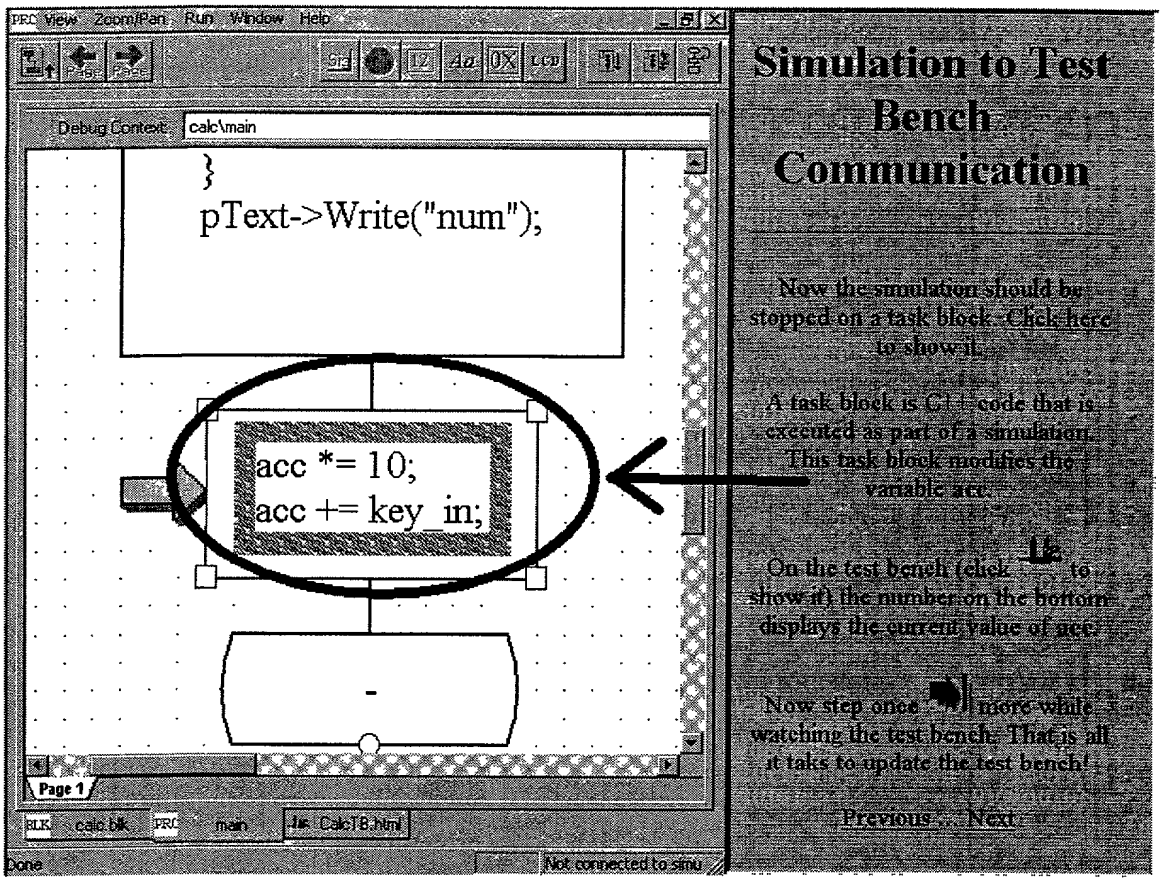

PRO View Zoom/Pan Run Window Help
Debug Context: calc\main
}
pText->Write("num");
acc *= 10;
acc += key_in;
-
Page 1
BLK calc.blk
PRO main
Calc18.Nmi
Done
Not connected to simu
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous Next

FIG. 49I

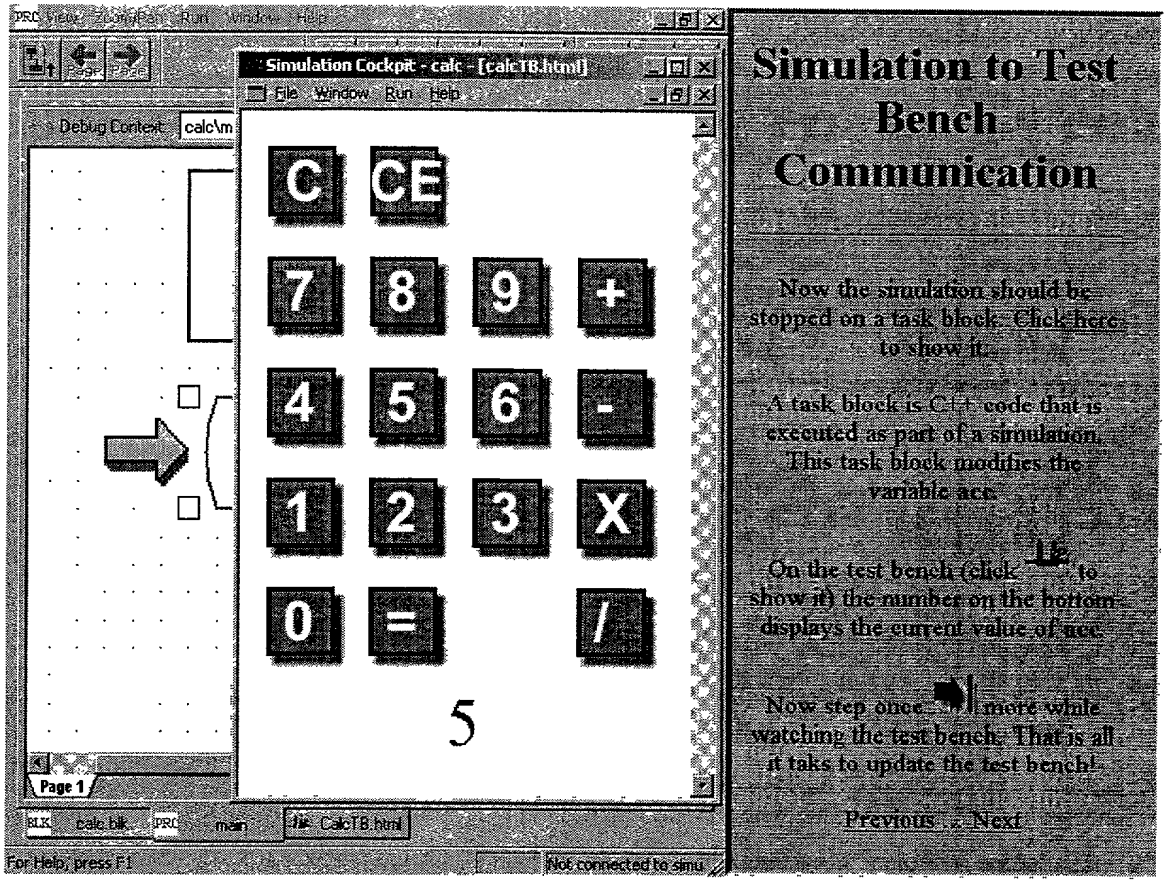
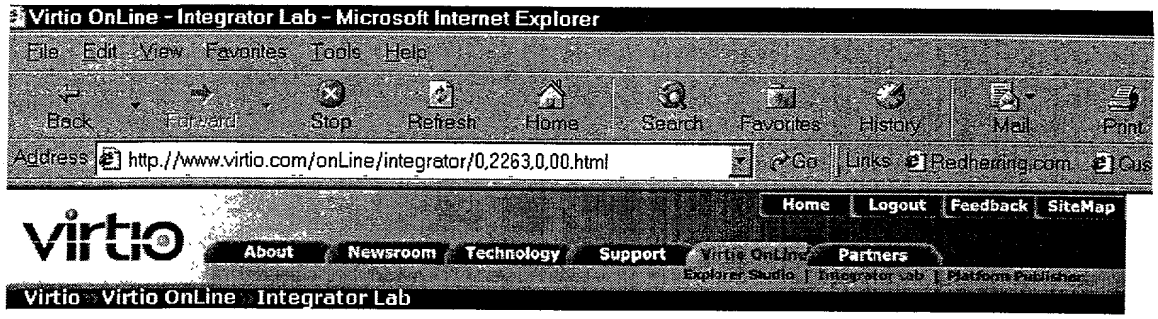

Simulation Cockpit - calc - [calcTB.html]
File Window Run Help
Debug Context
C CE
7 8 9 +
4 5 6 -
1 2 3 X
0 = /
5
Page 1
calc.blk
main
calcTB.html
For Help, press F1
Not connected to simu
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous Next

FIG. 49J

Integrator Lab Screen Snap Shots – On-Line Enablement



Integrator Lab

Current Designs | Browse IP

Design Name	Creation Date	Last Edit Date	Description	Delete Project
test	02-May-01	29-May-01	test	Delete
pcnetlink	04-May-01	25-May-01	asdasd	Delete
clonetutorial	23-May-01	23-May-01	testing cloning of build77	Delete
clonehanoi	25-Apr-01	31-May-01	cloning hanoi	Delete
cloneatlas	25-Apr-01	29-May-01	cloning atals	Delete

New Design

My Invitees

FIG. 50

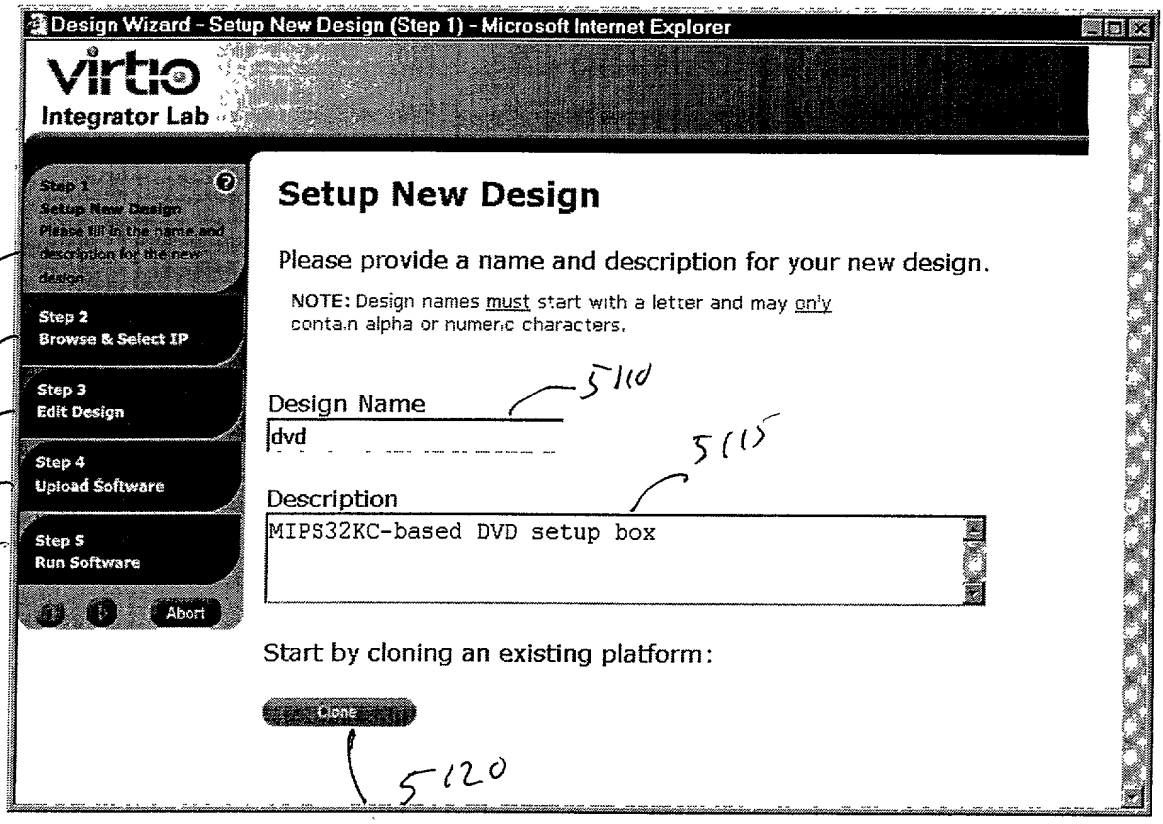

Design Wizard - Setup New Design (Step 1) - Microsoft Internet Explorer
virtio
Integrator Lab
Step 1
Setup New Design
Please fill in the name and description for the new design
Step 2
Browse & Select IP
Step 3
Edit Design
Step 4
Upload Software
Step 5
Run Software
Abort
Setup New Design
Please provide a name and description for your new design.
NOTE: Design names must start with a letter and may only contain alpha or numeric characters.
Design Name
dvd
Description
MIPS32KC-based DVD setup box
Start by cloning an existing platform:
Clone
5105
5102
5110
5115
5120

FIG. 51

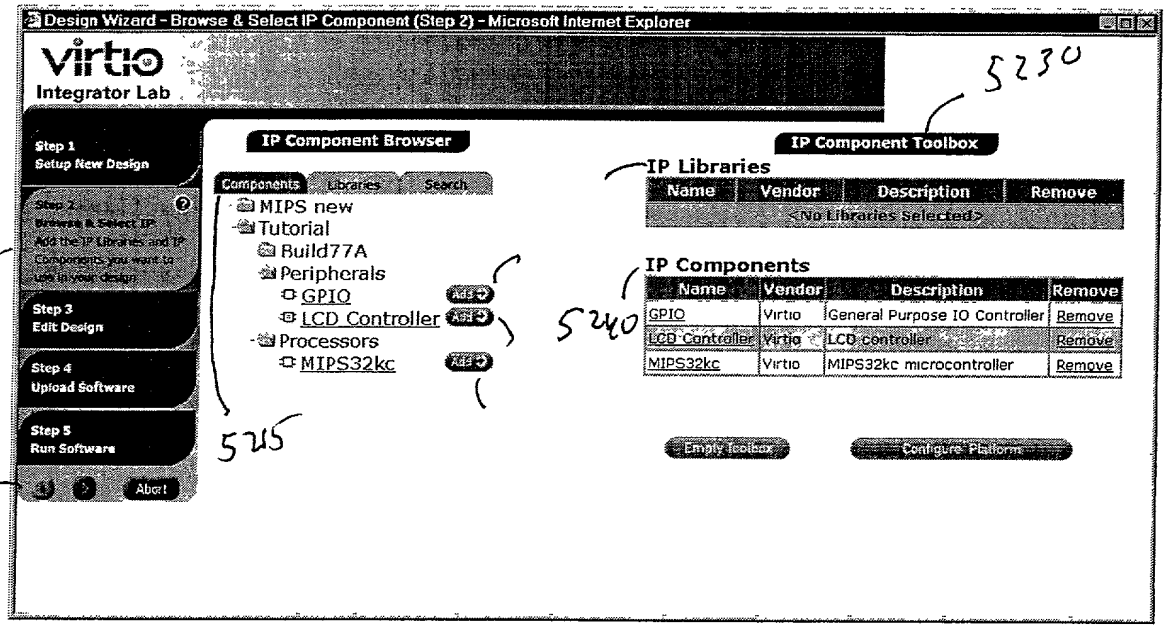

Design Wizard - Browse & Select IP Component (Step 2) - Microsoft Internet Explorer
virtio
Integrator Lab
Step 1
Setup New Design
Step 2
Browse & Select IP
Add the IP Libraries and IP Components you want to use in your design
Step 3
Edit Design
Step 4
Upload Software
Step 5
Run Software
Abort
IP Component Browser
Components
Libraries
Search
MIPS new
Tutorial
Build77A
Peripherals
GPIO
LCD Controller
Processors
MIPS32kc
Add
IP Component Toolbox
IP Libraries
Name
Vendor
Description
Remove
<No Libraries Selected>
IP Components
Name
Vendor
Description
Remove
GPIO
Virtio
General Purpose IO Controller
Remove
LCD Controller
Virtio
LCD controller
Remove
MIPS32kc
Virtio
MIPS32kc microcontroller
Remove
Empty Toolbox
Configure Platform
5202
5102
5205
5230
5240

FIG. 52

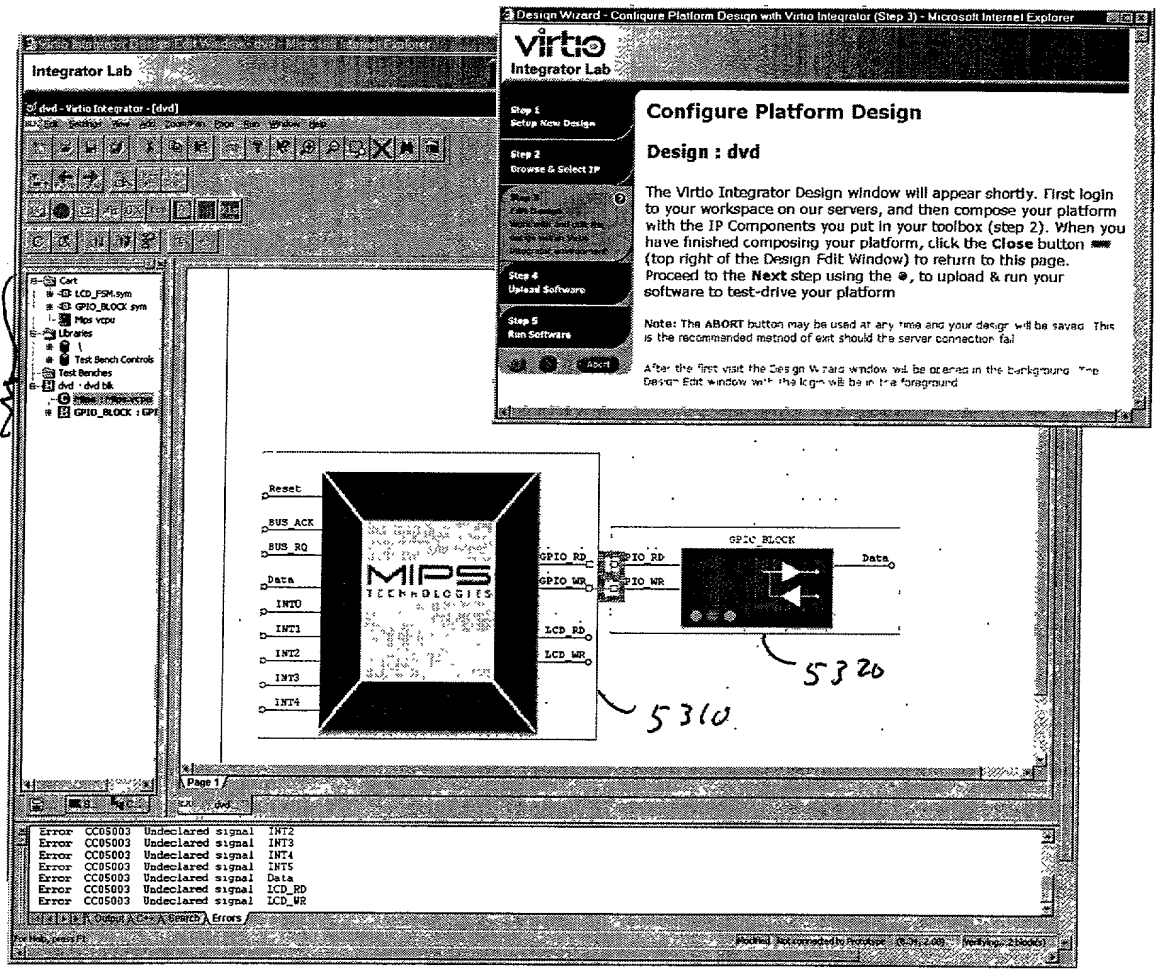
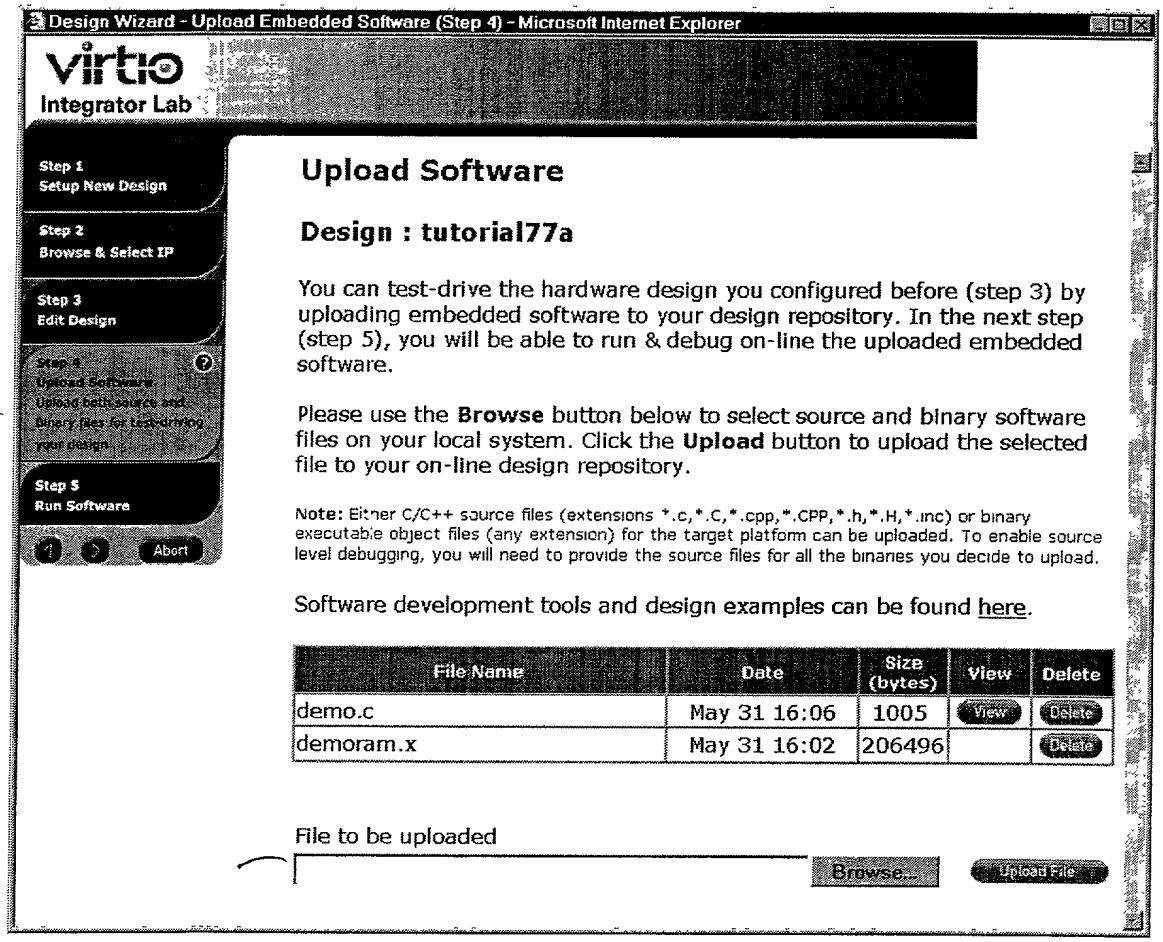

Design Wizard - Configure Platform Design with Virtio Integrator (Step 3) - Microsoft Internet Explorer
Integrator Lab
Configure Platform Design
Design : dvd
The Virtio Integrator Design window will appear shortly. First login to your workspace on our servers, and then compose your platform with the IP Components you put in your toolbox (step 2). When you have finished composing your platform, click the Close button (top right of the Design Edit Window) to return to this page. Proceed to the Next step using the , to upload & run your software to test-drive your platform
Note: The ABORT button may be used at any time and your design will be saved. This is the recommended method of exit should the server connection fail
Step 1 Setup New Design
Step 2 Browse & Select IP
Step 4 Upload Software
Step 5 Run Software
Abort
Reset
BUS_ACK
BUS_RQ
Data
INT0
INT1
INT2
INT3
INT4
GPIO_RD
GPIO_WR
LCD_RD
LCD_WR
MIPS TECHNOLOGIES
GPIO_BLOCK
Data
5305
5310
5320
Error CC05003 Undeclared signal INT2
Error CC05003 Undeclared signal INT3
Error CC05003 Undeclared signal INT4
Error CC05003 Undeclared signal INT5
Error CC05003 Undeclared signal Data
Error CC05003 Undeclared signal LCD_RD
Error CC05003 Undeclared signal LCD_WR

FIG. 53


Design Wizard - Upload Embedded Software (Step 4) - Microsoft Internet Explorer
virtio
Integrator Lab
Step 1
Setup New Design
Step 2
Browse & Select IP
Step 3
Edit Design
Step 4
Upload Software
Upload both source and
Binary files for test-driving
your design
Step 5
Run Software
Abort
Upload Software
Design : tutorial77a
You can test-drive the hardware design you configured before (step 3) by uploading embedded software to your design repository. In the next step (step 5), you will be able to run & debug on-line the uploaded embedded software.
Please use the Browse button below to select source and binary software files on your local system. Click the Upload button to upload the selected file to your on-line design repository.
Note: Either C/C++ source files (extensions *.c,*.C,*.cpp,*.CPP,*.h,*.H,*.inc) or binary executable object files (any extension) for the target platform can be uploaded. To enable source level debugging, you will need to provide the source files for all the binaries you decide to upload.
Software development tools and design examples can be found here.
File Name
Date
Size (bytes)
View
Delete
demo.c
May 31 16:06
1005
View
Delete
demoram.x
May 31 16:02
206496
Delete
File to be uploaded
Browse...
Upload File

5405

FIG. 54

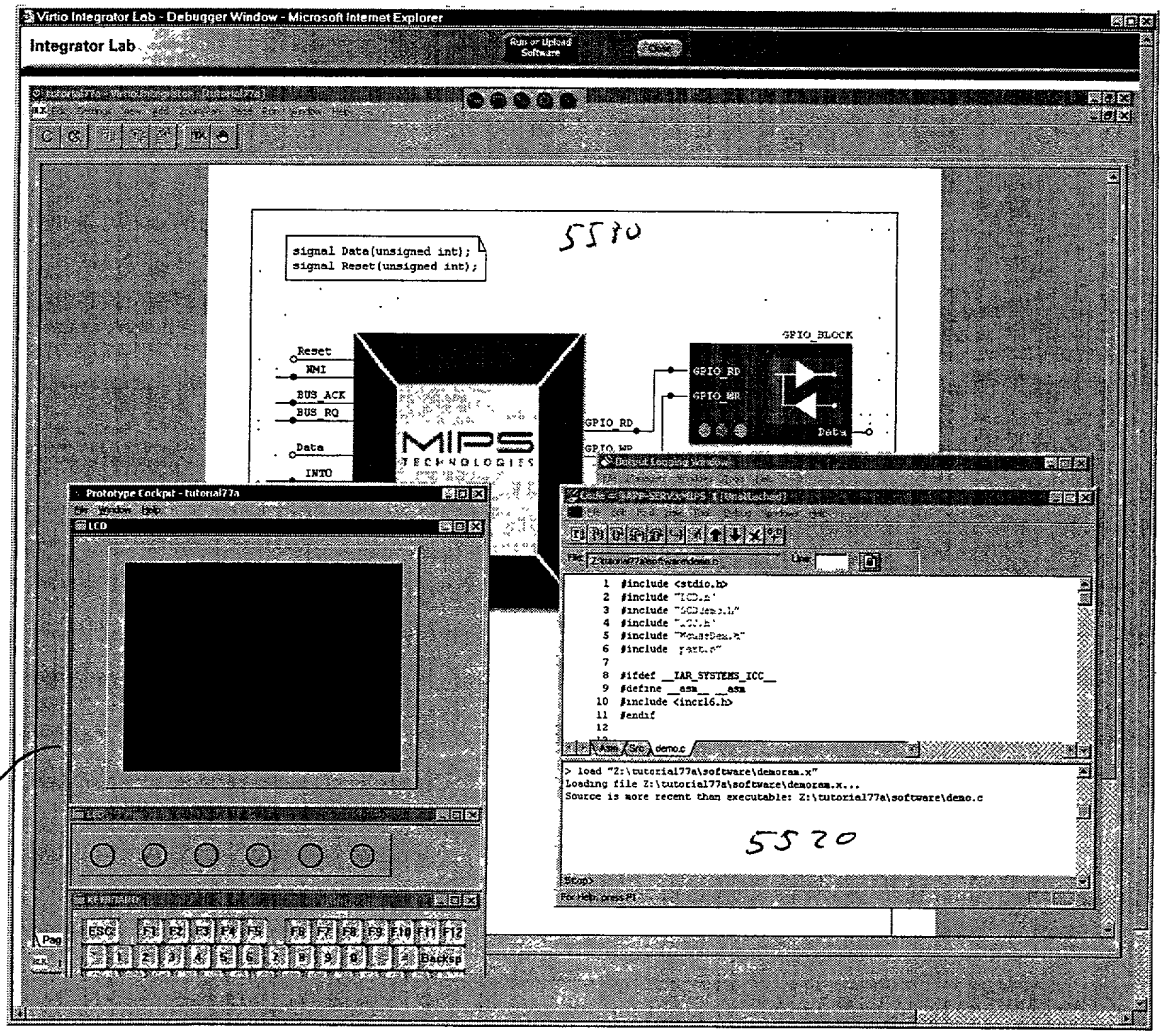

Virtio Integrator Lab - Debugger Window - Microsoft Internet Explorer
Integrator Lab
5530
signal Data(unsigned int);
signal Reset(unsigned int);
Reset
NMI
BUS_ACK
BUS_RQ
Data
INTO
MIPS
TECHNOLOGIES
GPIO_BLOCK
GPIO_RD
GPIO_WR
Data
Prototype Cockpit - tutorial77a
LCD
5510
#include <stdio.h>
#include "ICD.h"
#include "SCDisp.h"
#include "_CJ.h"
#include "MouseDem.h"
#include "part.h"
#ifdef __IAR_SYSTEMS_ICC__
#define __asm__ asm
#include <incr16.h>
#endif
demo.c
> load "Z:\tutorial77a\software\demoram.x"
Loading file Z:\tutorial77a\software\demoram.x...
Source is more recent than executable: Z:\tutorial77a\software\demo.c
5520

FIG. 55